ESC-TR-97-097

Quarterly Technical Report

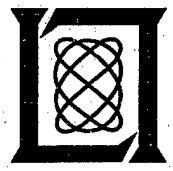
Solid State Research

1997:4

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LEXINGTON, MASSACHUSETTS



Prepared for the Department of the Air Force under Contract F19628-95-C-0002.

Prepared with partial support of the Department of the Air Force under Contract F19628-95-C-0002.

The ESC Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

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FOR THE COMMANDER

Gary Tatungian
Administrative Contracting Officer
Directorate of Contracted Support Management

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 AUGUST – 31 OCTOBER 1997

ISSUED 22 APRIL 1998

LEXINGTON MASSACHUSETTS

ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 August through 31 October 1997. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, High Speed Electronics, Microelectronics, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

Up to 40-W CW of linearly polarized output has been demonstrated from a Yb:YAG laser in which the gain element is cooled to near liquid-nitrogen temperatures. No thermo-optic effects have been observed in this laser.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

GaInAsSb epilayers, lattice matched to GaSb substrates, have been grown by organometallic vapor phase epitaxy (OMVPE) using a novel combination of precursors including triethylgallium, trimethylindium, tertiarybutylarsine, and trimethylantimony. The new combination demonstrated improved material qualities over conventional precursors.

GaInAsSb epilayers grown by OMVPE have been doped *p*- and *n*-type. The *p*-type doping was in the range 10^{16}–10^{18} cm^{-3} with dimethylzinc, and the *n*-type doping in the range 10^{17}–10^{18} cm^{-3} with diethyltellurium.

3. SUBMICROMETER TECHNOLOGY

The trilayer resist geometry has been used as an experimental vehicle to study the mechanisms and magnitude of line edge roughness (LER) in top-surface imaging and multilayer resist systems. A statistical experimental design was used to optimize plasma etch conditions in order to minimize sidewall and LER.

4. HIGH SPEED ELECTRONICS

An integrated-microvalve technique using elastic-membrane microvalves has been developed and tested. An integrated-microvalve technology is a critical key to achieving microfluidic systems of useful complexity.

5. MICROELECTRONICS

A high-quantum-efficiency and low-noise 640 × 480-pixel digital camera system, operating at 30 frames per second, has been developed for nighttime imaging applications. Experimental results, both in the laboratory under controlled illumination and in the field under natural lighting, show that the camera system has useful sensitivity below starlight illumination levels.

6. ANALOG DEVICE TECHNOLOGY

A model has been developed for resistor fabrication in a low-temperature superconducting electronics process. The resistors are used for precise control of circuit elements in the operation of low-temperature, Josephson junction-based, superconducting monolithic circuits at clock speeds approaching 50 GHz.

7. ADVANCED SILICON TECHNOLOGY

A program has begun to build MOSFETs with 25-nm channel length, about 10 times smaller than today's advanced devices. The device concept has been developed, simulations have been done, and experiments have been performed on phase-shift optical lithography, a TiN midgap gate, and a damascene process for producing sub-50-nm gates.

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Diamond Cold Cathodes	M. W. Geis J. C. Twichell T. M. Lyszczarz K. E. Krohn N. N. Efremow	American Vacuum Society Meeting, San Jose, California, 20-24 October 1997

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1. QUANTUM ELECTRONICS

1.1 COOLED Yb:YAG LASERS

Yb:YAG lasers at 1.03 μm have the potential for high-average-power operation while maintaining good beam quality by virtue of the relatively low thermal loading in the gain medium [1]. It was recently recognized that the average powers could be even higher if the Yb:YAG were to be cooled to cryogenic temperatures [2] because of the significantly larger thermal conductivity and smaller thermal expansion and *dn/dT* of YAG. Here, initial experiments are reported in a Yb:YAG laser that has a cooled gain element. The results show that thermo-optic effects are negligible to the tens of watts output power level.

A schematic of the laser is shown in Figure 1-1. The Yb:YAG gain element consists of 0.5 cm of 4%-doped Yb:YAG with diffusion-bonded end caps of undoped YAG of 0.25-mm thickness. The ends are antireflection coated for 1.0-μm wavelength with a single quarter-wave of MgF_2. This gain element is In-bonded to a Cu holder which attaches to the cold finger of a LN_2 dewar. The gain element is end pumped from each end by the output from a fiber-coupled, CW InGaAs diode array, each capable of delivering up to ~60-W CW output power at 0.94 μm. The fibers have a core diameter of 0.216 cm and a numerical aperture of 0.12. The output from the fiber is imaged 1:1 into the Yb:YAG gain element. The laser resonator is nearly hemispherical with a 50-cm radius of curvature high reflector and a 60-cm radius of curvature output coupler and a physical cavity length of 104.5 cm, with two flat folding mirrors inside the resonator for convenience. The output coupler has a transmission of 25% which gives the most optimum output coupling among couplers with 2, 5, and 50% transmission. A Brewster-angle window could be inserted into the resonator in order to force the output to be linearly polarized; otherwise the laser operated with unpolarized output.

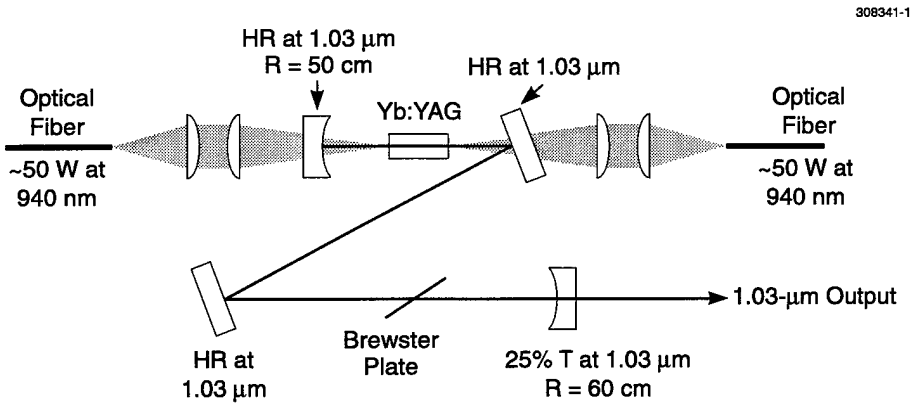

Figure 1-1. Schematic of laser resonator.

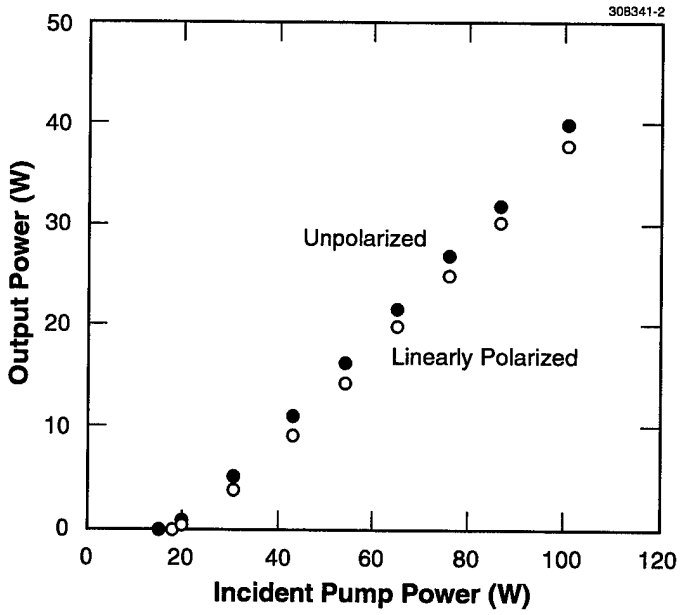

Figure 1-2. Output power at 1.03 μm as a function of 0.94-μm pump power incident on the dewar windows for unpolarized and linearly polarized operation.

The laser results are shown in Figure 1-2. A linearly polarized (polarization ratio of ~100:1) output power of nearly 40 W was obtained for an incident power (incident on the dewar windows) of 100 W; the output power was limited by the power supplies driving the diode laser arrays. The slope efficiency for the polarized output was 49% relative to incident power. The fact that the unpolarized output is only slightly higher at all output power levels than the linearly polarized output shows that stress-induced birefringence in the Yb:YAG rod is negligible. Beam quality measurements were made at the highest output power and at 15 W. The beam quality was approximately the same at the two output powers with an M^2 of ~2, indicating that thermo-optic distortions are sufficiently small that they have no effect at these power levels. A measurement of thermal lensing was attempted but no focusing was observed; given the sensitivity of the measurement, the focal length of the thermal lens was >10 m.

T. Y. Fan

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 OMVPE GROWTH OF GaInAsSb IN THE RANGE 2–2.4 μm

$Ga_{1-x}In_xAs_ySb_{1-y}$ is an important material for optoelectronic devices such as lasers [1], detectors [2], and thermophotovoltaics [3] that operate in the mid infrared. This alloy can be lattice matched to GaSb or InAs substrates and has a direct energy gap adjustable in the wavelength range 1.7 μm (0.726 eV) to 4.2 μm (0.296 eV). In previous reports on growth of GaInAsSb by organometallic vapor phase epitaxy (OMVPE), alloys were grown with trimethylgallium (TMGa) as the gallium precursor [4]–[8]. For growth temperatures which ranged between 500 and 550°C, TMGa was not completely pyrolized [4],[7] and the composition of In in the alloy was found to be dependent on growth temperature. Although precursor decomposition is reactor and pressure dependent, we similarly determined GaSb growth is kinetically limited below 640°C for TMGa and trimethylantimony (TMSb), but that it is mass transport limited between 525 and 640°C when triethylgallium (TEGa) is used [9]. Thus, there is a potential advantage to using TEGa as the gallium precursor for growth of GaInAsSb. Here, we report OMVPE growth of $Ga_{1-x}In_xAs_ySb_{1-y}$ alloys lattice matched to GaSb with TEGa, trimethylindium (TMIn), tertiarybutylarsine (TBAs), and TMSb.

GaInAsSb epitaxial layers were grown on (100) GaSb substrates, oriented 2° toward (110) in a vertical rotating-disk reactor operating at 150 Torr with H_2 as the carrier gas. Solution TMIn, TEGa, TBAs, and TMSb were used as organometallic precursors. Solution TMIn and TEGa were maintained at 24°C, TMSb at 0°C, and TBAs at –8°C. The total group III mole fraction was typically $3.5–4 \times 10^{-4}$, which resulted in a growth rate of ~2.5–2.7 μm/h. The V/III ratio ranged from 0.9 to 1.7. The TMIn fraction in the gas phase, $p_{TMIn}/[p_{TMIn} + p_{TEGa}]$, was varied from 0.127 to 0.267. For lattice matching to GaSb substrates, the TBAs fraction in the gas phase, $p_{TBAs}/[p_{TBAs} + p_{TMSb}]$, was varied from 0.05 to 0.15. The growth temperature was varied from 525 to 575°C.

The surface morphology was examined by means of Nomarski contrast microscopy. Double-crystal x-ray diffraction (DCXD) was used to measure the degree of lattice mismatch $\Delta a/a$ to GaSb substrates. Photoluminescence (PL) was measured at 300 K using a PbS detector. The In and As content of epilayers was determined from DCXD splitting, the peak emission in 300-K PL spectra, and the energy gap dependence on composition based on the binary bandgaps [10]: $E(x,y) = 0.726 - 0.961x - 0.501y + 0.08xy + 0.415x^2 + 1.2y^2 + 0.021x^2y - 0.62xy^2$. For alloys lattice matched to GaSb, $y = 0.867(x)/(1 - 0.048x)$.

The surface morphology of GaInAsSb layers depends on V/III ratio, In content, and growth temperature. Figure 2-1 shows the surface morphology of $Ga_{0.88}In_{0.12}As_{0.1}Sb_{0.9}$ layers grown with various V/III ratios at 575°C on GaSb substrates. The layers are nominally lattice matched to the GaSb substrate ($\Delta a/a < 1.5 \times 10^{-3}$). For V/III = 0.9, the surface is metal-rich and hazy to the naked eye. When the V/III ratio was increased to 1.05, the surface morphology is mirror-like. As the V/III ratio was increased further, however, Nomarski contrast microscopy revealed surface texture which increases with V/III ratio. These results are similar to the morphology dependence on V/III ratio observed for GaSb [9]. When the growth temperature

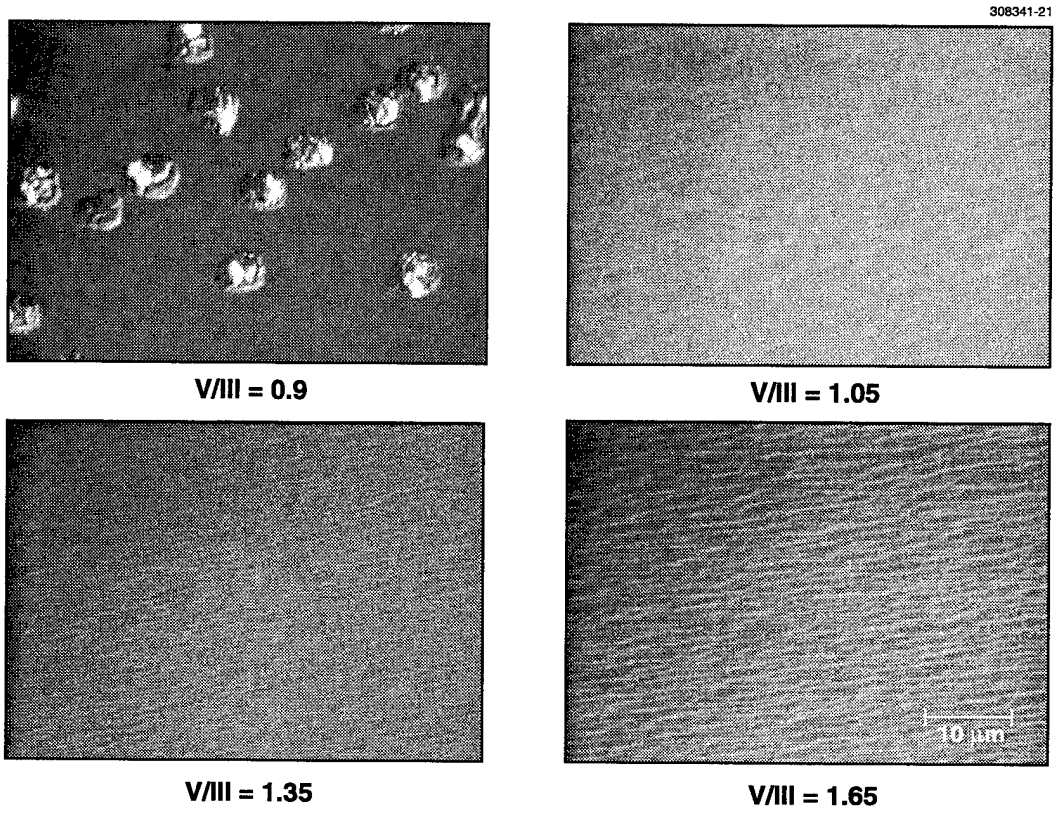

Figure 2-1. Surface morphology of GaInAsSb epilayers grown on GaSb at 575°C and various V/III ratios.

was reduced to 550 and 525°C, the minimum V/III ratio increased to 1.15 and 1.25, respectively. We also observed that GaInAsSb layers of similar composition exhibit a smoother morphology when those layers are grown at a lower temperature of 550 or 525°C compared to 575°C. The surface morphology also depends on the In content. For layers with lower In concentration (i.e., composition moving away from the GaSb corner of the miscibility phase diagram [4]), the surface becomes smoother, and for $Ga_{0.9}In_{0.1}As_{0.08}Sb_{0.92}$, a mirror smooth surface could be obtained for epilayers grown at a growth temperature of 550°C.

The distribution coefficient of In is shown in Figure 2-2. The data are plotted for layers grown at 525, 550, or 575°C. The V/III ratio ranged between 1.1 and 1.3. For these layers, $|\Delta a/a| < 2 \times 10^{-3}$. The In distribution coefficient is 1.2 at 525°C, and decreases to 0.95 and 0.5 for 550 and 575°C, respectively. The trend of a lower In distribution coefficient with increasing temperature is similar to results reported for growth using TMGa and TMIn [4],[7]. However, in those studies, the dependence is attributed to the increase in TMGa pyrolysis with temperature. For the range of growth temperatures and reactor used in

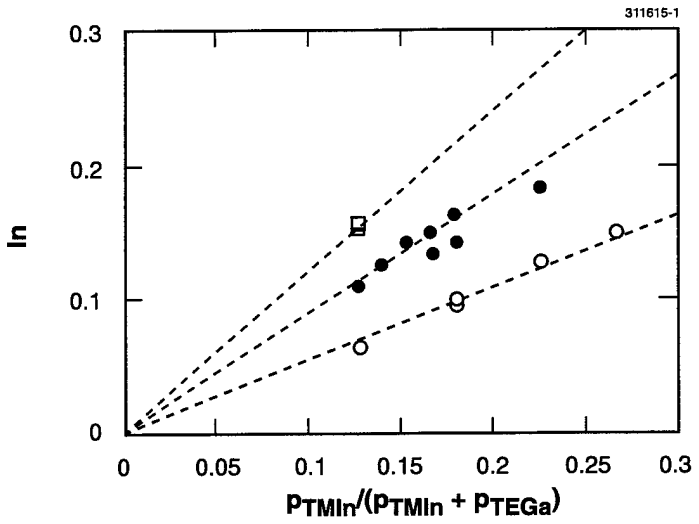

Figure 2-2. Distribution coefficients of In for GaInAsSb grown nominally lattice matched to GaSb at 525°C (open squares), 550°C (solid circles), and 575°C (open circles).

this study, it is likely that both TMIn and TEGa are completely pyrolyzed. Thus, these results are somewhat surprising and may reflect a difference in surface kinetics.

The distribution coefficient of As is shown in Figure 2-3. It is approximately unity independent of growth temperature, indicating complete pyrolysis of TBAs and TMSb. This result is somewhat surprising since we concluded from growth studies of GaSb with TEGa and TMSb that a temperature of 600°C is required to completely pyrolyze TMSb in our vertical reactor [9]. The decomposition of TMSb may be enhanced by the presence of the other precursors used in this study. In contrast, the As distribution coefficient was reported to be a strong function of temperature when TMGa, TMIn, TBAs, and TMSb were used as precursors [7].

The degree of lattice mismatch of GaInAsSb epilayers on GaSb can influence the performance of minority carrier-type devices, such as thermophotovoltaics [3]. Therefore, we determined the sensitivity of lattice mismatch on the fraction of TBAs in the gas phase. Figure 2-4 shows the lattice mismatch as a function of TBAs fraction for layers grown at 575°C and group III mole fraction of 4×10^{-4}. The lattice mismatch variation is about 1.5×10^{-3} per % TBAs fraction, which corresponds to about 160 arc sec per sccm H_2 flow through the TBAs bubbler. Since the reproducibility of a typical mass flow controller is 0.1 sccm, the data indicate TBAs can be used to provide excellent controllability of lattice-matching conditions.

For electrical characterization, GaInAsSb was grown at 550°C on semi-insulating (SI) (100) GaAs substrates misoriented 2° toward (110), since SI GaSb substrates are not available. Carrier concentration

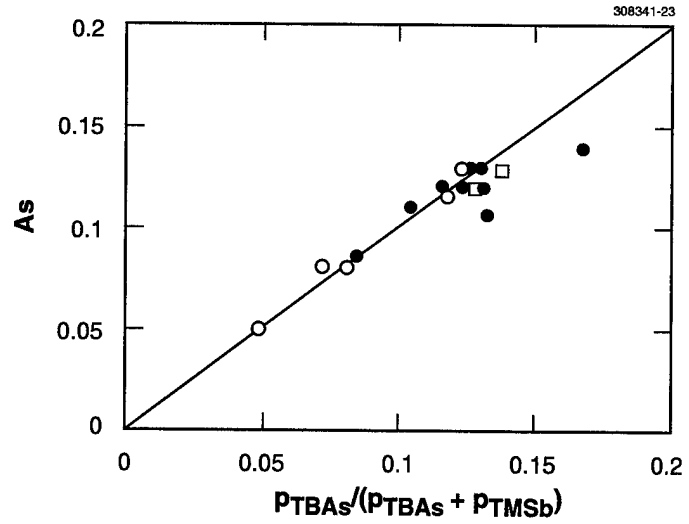

Figure 2-3. Distribution coefficient of As for GaInAsSb grown nominally lattice matched to GaSb at 525°C (open squares), 550°C (solid circles), and 575°C (open circles).

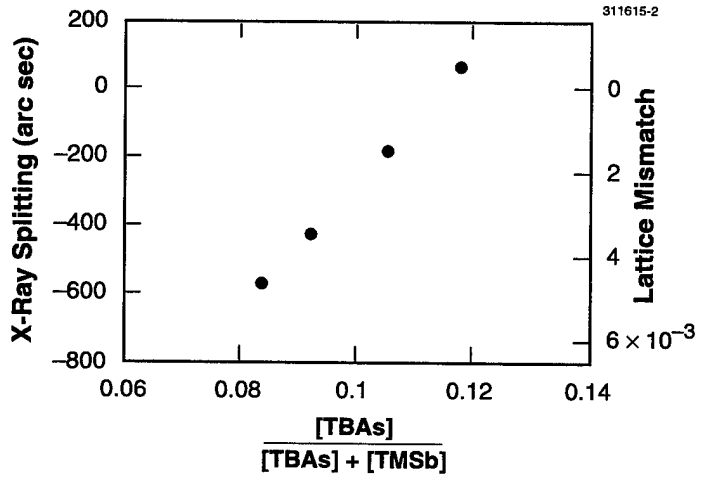

Figure 2-4. Lattice mismatch of GaInAsSb grown at 575°C as a function of TBAs fraction in the gas phase.

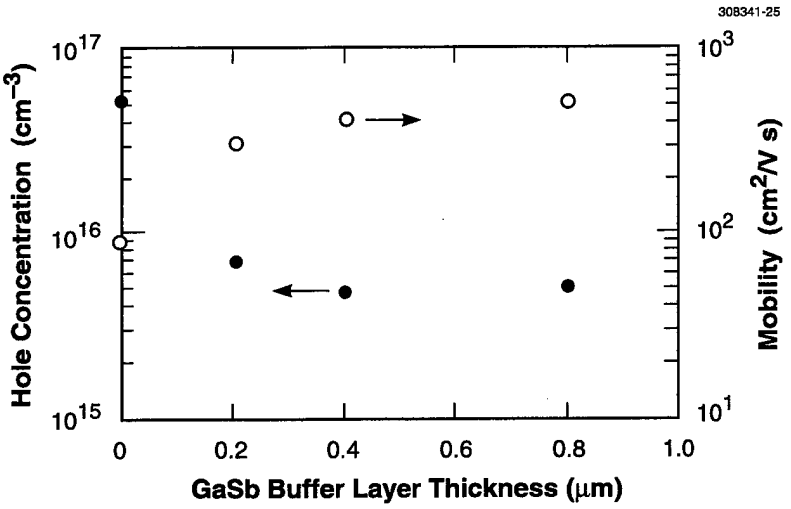

Figure 2-5. Electrical properties of GaInAsSb grown at 550°C as a function of GaSb buffer layer thickness.

and mobility of GaInAsSb epilayers, which were grown about 3 μm thick, were obtained from Hall measurements based on the van der Pauw method. Since the lattice mismatch between GaInAsSb (lattice matched to GaSb) and GaAs is 8%, misfit dislocations are generated and propagate through the GaInAsSb epilayer [11]. These defects can be electrically active, but can be mitigated by the growth of a buffer layer [12]. Therefore, a GaSb buffer layer was first grown on the GaAs substrate at 550°C. The growth rate of the buffer layer was ~1 μm/h. The electrical properties measured at 300 K of nominally undoped $Ga_{0.84}In_{0.14}As_{0.12}Sb_{0.88}$ layers grown at 550°C are shown in Figure 2-5 as a function of GaSb buffer layer thickness. All layers are *p*-type with hole concentration (mobility) decreasing (increasing) with GaSb buffer layer thickness. Without a buffer layer the hole concentration is as high as 5×10^{16} cm^{-3}, and decreases by an order of magnitude when the buffer layer is 0.4 μm or greater. The mobility is as low as 90 cm^2/V s without the buffer compared to 560 cm^2/V s with a 0.8-μm-thick GaSb buffer layer. Considerably higher hole concentration and lower hole mobility values were recently reported for GaInAsSb grown with TMGa, TMIn, arsine, and TMSb [12]. The hole concentration was $2–5 \times 10^{16}$ cm^{-3} and mobility 220–320 cm^2/V s. For GaInAsSb layers grown by molecular beam epitaxy (MBE), the hole concentration was reported to be $4–5 \times 10^{16}$ cm^{-3} and mobility 254 cm^2/V s [13].

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2.2 ZINC AND TELLURIUM DOPING OF GaInAsSb

Previously, we discussed the growth of GaInAsSb in the range 2–2.4 μm by OMVPE [14]. Here, we report the *p*- and *n*-type doping of these epilayers. GaInAsSb layers were grown on (100) SI GaAs substrates, oriented 2° toward (110) or 6° toward (111)B as previously described. GaAs substrates were used since SI GaSb substrates are not available. Diethyltellurium DETe (10 ppm in H_2) and dimethylzinc (DMZn) (1000 ppm in H_2) were used as the *n*- and *p*-type doping sources, respectively. The growth temperature was 550°C. Since the mismatch between GaInAsSb and GaAs is 8%, a 0.4-μm-thick GaSb buffer layer was first grown to reduce the contribution of electrically active defects due to the lattice mismatch.

The hole concentration plotted as a function of the DMZn mole fraction is shown in Figure 2-6 for $Ga_{0.87}In_{0.13}As_{0.12}Sb_{0.88}$ layers grown on the two different substrate misorientations. The hole concentration increases linearly with DMZn mole fraction 7.5–80 $\times 10^{-7}$, and ranges from 6.3×10^{16} to 8.9×10^{17} cm^{-3} for (100) 2° toward (110) substrates and from 9.5×10^{16} to 1.7×10^{18} cm^{-3} for (100) 6° toward (111)B. The hole concentration is 1.5–1.6 times greater for layers grown on (100) substrates with a 6° toward (111)B misorientation compared to the 2° toward (110) misorientation, which suggests that there is a preferential incorporation of Zn on the 6° toward (111)B misorientation. This may result from the higher density of Sb and As dangling bonds on the 6° toward (111)B misorientation substrate compared to the 2° toward (110) misorientation. Zn substitutionally occupies a group III site. Thus, the number of available sites for Zn adsorption increases with group V dangling bonds. Similarly, it is expected that an increase in TMSb exposure will increase Zn incorporation. In a separate set of experiments with constant DMZn mole fraction, the TMSb was varied from 3.2 to 3.5×10^{-4} mole fraction. The corresponding hole concentration increased 1.7 times for both substrate misorientations, which is consistent with the mechanism suggested for the Zn incorporation.

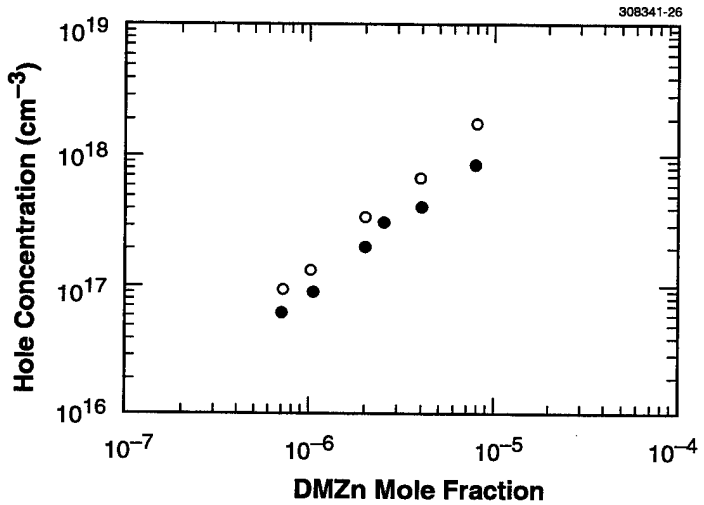

Figure 2-6. Hole concentration as a function of dimethylzinc mole fraction in the gas phase. Closed circles are on (100) 2° toward (110) and open circles on (100) 6° toward (111) B substrates.

Figure 2-7 shows the electron concentration plotted as a function of the DETe mole fraction. The electron concentration ranges from 2.7×10^{17} to 2.3×10^{18} cm^{-3} for the 2° toward (110) misorientation and 2.3×10^{17} to 2.05×10^{18} cm^{-3} for the 6° toward (111)B misorientation. Compared to Zn incorporation, Te incorporation appears to be less sensitive to substrate misorientation since the electron concentration is 0.86 to 0.9 times lower for the 6° toward (111)B misorientation compared to the 2° toward (110) misorientation. Since Te is likely to sit on a group V site, its adsorption on the (100) 6° toward (111)B substrate may be reduced compared to (100) 2° toward (110). When the TMSb mole fraction was increased from 3.4 to 3.7×10^{-4}, the electron concentration decreased about 0.85 times.

The 300-K electrical properties of *p*- and *n*-doped $Ga_{1-x}In_xAs_ySb_{1-y}$ ($x \sim 0.13$, $y \sim 0.12$) are summarized in Figures 2-8 and 2-9, respectively. With one exception, the data are plotted for GaInAsSb grown on a 0.4-μm-thick buffer layer (see Figure 2-3). The hole concentration ranged from 4.4×10^{15} to 1.7×10^{18} cm^{-3} with mobility values between 560 and 180 cm^2/V s, respectively. The open circle represents the result obtained for GaInAsSb grown on a 0.8-μm-thick buffer layer. Thus, these mobility values are likely to be an underestimate of values that would be measured for bulk material, since the lattice mismatch is significant, and we have not tried to optimize the GaSb buffer layer growth. The electron concentration ranged from 2.3×10^{17} to 2.3×10^{18} cm^{-3}, with corresponding mobility values between 5208 and 2084 cm^2/V s, respectively. Although there are extremely limited data for GaInAsSb electrical properties [5],[12],[13], we believe these results are a significant improvement over results reported previously for GaInAsSb layers of similar composition grown either by OMVPE [5],[12] or MBE [13]. In those reports, a hole concentration

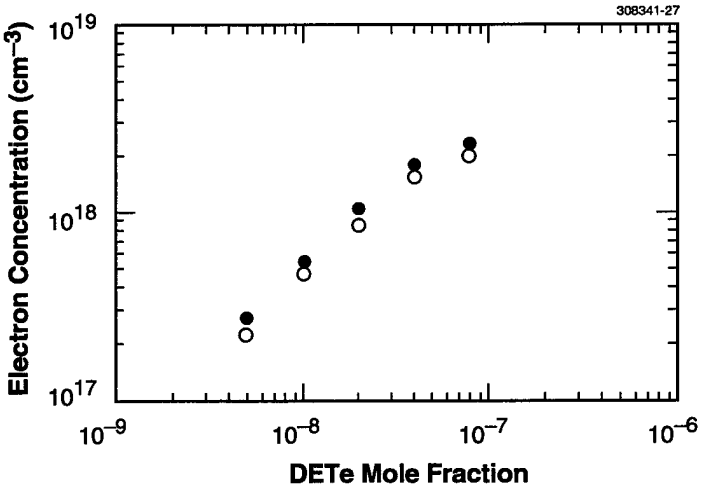

Figure 2-7. Electron concentration as a function of diethyltellurium mole fraction in the gas phase. Closed circles are on (100) 2° toward (110) and open circles on (100) 6° toward (111) B substrates.

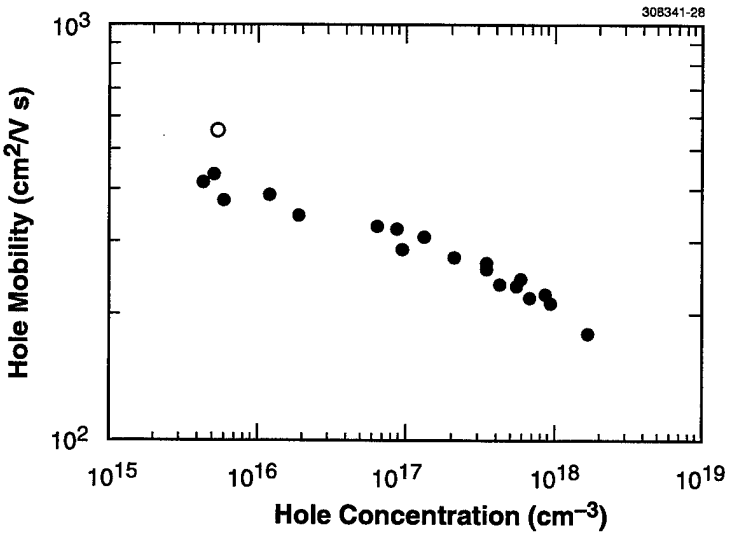

Figure 2-8. Electrical properties of p-GaInAsSb. Closed circles represent data with 0.4-μm-thick GaSb buffer layer and open circle with 0.8-μm-thick buffer layer.

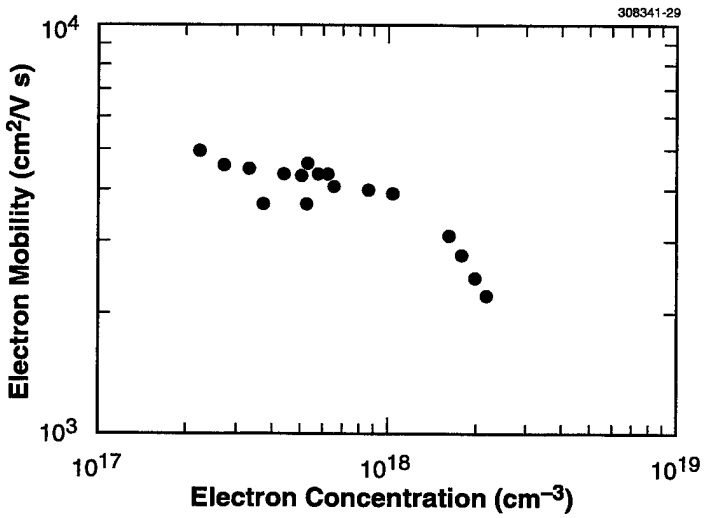

Figure 2-9. Electrical properties of n-GaInAsSb.

of 2–5 × 10^{16} cm^{-3} with mobility values between 220 and 320 cm^2/V s was reported for OMVPE-grown GaInAsSb [12], and an electron concentration of 1 × 10^{17} cm^{-3} with a corresponding mobility value of 2620 cm^2/V s for MBE-grown GaInAsSb [13].

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3. SUBMICROMETER TECHNOLOGY

3.1 PLASMA-INDUCED ROUGHNESS IN TRILAYER RESIST ETCHING

Plasma-induced formation of surface, sidewall, and line-edge roughness (LER) on the nanometer scale will impact the ultimate resolution of resists and patterned features. Dry-developed resists, both top-surface imaging (TSI) and multilayer resists, exhibit an inherent LER which results from erosion of both the etch mask—in situ dry-developed organosilicon for TSI, and deposited hardmask for trilayer—and the underlying resist. As part of a Sematech project to delineate the mechanism and magnitude of LER for TSI, we are investigating the mechanistic effects of various etch parameters, such as ion energy, ambient pressure, and temperature, on the formation of edge roughness.

The trilayer process, shown schematically in Figure 3-1, with a separately patterned plasma-enhanced chemical vapor deposition (PECVD) oxide hardmask, represents an ideal, high-contrast, silicon-containing etch mask, which because of its high silicon content is less sensitive to edge erosion and faceting during reactive ion etching (RIE). As such it can be used to separate LER caused by mask erosion and mask edge faceting from that caused by plasma-induced sidewall roughness in the undercoat resist layer. In addition, it can be used to optimize etching conditions for the resist profile independently of the silylation mask shape.

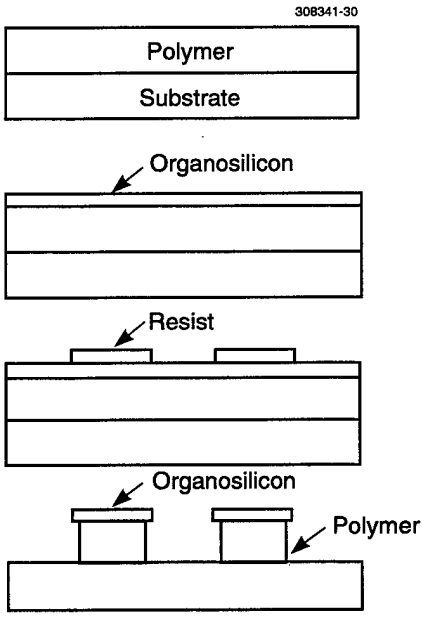


Figure 3-1. Schematic of trilayer resist process. For these experiments, patterned trilayers were prepared consisting of a 1.1-μm-thick fusion baked novolac planarizing layer, a 0.2-μm-thick PECVD SiO_2 hardmask, and a 0.7-μm-thick UV-4 resist imaging layer.

A low-pressure, high-density plasma source, such as a transformer-coupled plasma (TCP) RIE system, provides independent control over the ion energy and ion flux arriving at the wafer surface [1]. Thus, it offers a platform for investigating how the mechanisms of ion bombardment and density of etchant species (reactive neutrals and ions) impact the evolution of edge, surface, and sidewall roughness. Ion bombardment, while necessary for high-fidelity and anisotropic pattern transfer, can cause a number of undesirable and detrimental effects. These include redeposition of involatile species by back sputtering of material from the bottom of the etched groove or forward sputtering of the mask material onto the sidewall of the etched grooves, faceting of the mask edge due to the angle-dependent sputter yield of the physical ion bombardment process, and ion scattering in the sheath which results in a distribution of the ion impingement angles and in hourglass-shaped etch profiles. These chemical and physical etching effects, observed in the various etched profiles, are discussed below.

Response surface methodology, a statistical experimental design technique, has been used to evaluate the effects of key process parameters while minimizing the number of experiments, and wafers, necessary to find the optimal etch conditions. A commercially available software package (JMP®) was used to generate the statistical design of experiments (SDE) shown in Table 3-1, a center composite orthogonal design composed of eight full factorial points, six center axial points, and six repeats of the center point. The SDE was designed to isolate the effects of three main variables—TCP source power (range 50–600 W), chuck bias power (range 50–380 W), and reactor pressure (2–5 mTorr)—on the profile and sidewall roughness. Earlier experiments demonstrated minimal lateral undercutting at low pressures, where the longer mean free path ensures high ion directionality and reduces ion angular-dependent scattering effects. While the 1000-l/s turbo pump on the TCP etcher limits the O_2 flow to 60 sccm for an operating pressure of ~2 mTorr, this is not a flow-rate-limited regime. Both patterned and blanket wafers have been etched and evaluated for etch rate, selectivity, profile, and to correlate surface roughening with edge and sidewall roughening. All experiments were conducted at –30°C, since previous experiments have demonstrated the reduction and/or elimination of lateral etching, attributed to a sidewall passivation layer formed by the freeze-out of OH complexes, CO, and CO_2 [2]–[4]. Randomized data have been collected at the points indicated by the experimental design. Resist etch rates were determined from blanket wafers using an imaging interferometric end point system, shown in Figure 3-2. This allowed us to calculate the etch rates and etch uniformity across a 6-in. wafer.

Cross sections of gold-coated etched profiles and high-resolution sidewall images of uncoated samples were evaluated by scanning electron microscopy (SEM). From these, it is apparent that the different etch conditions yield a number of very different profiles and resist sidewall morphologies. Responses studied included the etch rate, the selectivity, the sidewall roughness, the 3σ uniformity, and the profile—whether it is undercut, inverted, or bowed. It is apparent from the profiles of dense vs isolated lines that whereas densely patterned lines exhibit no undercut at the mask/resist interface but have bow, the isolated lines show an undercut and no apparent bow. The location of the minimum bow on the dense lines is a function of the three process variables—TCP source power, chuck bias power, and pressure. In addition, the amount of bow and the amount of reduction of the bottom width on both isolated lines and gratings are

TABLE 3-1
Statistical Design of Experiment

Pattern	Block	Source Power (W)	Chuck Power (W)	Pressure (mTorr)	Comment
− − −	1	150	100	2.5	Full factorial
− − +	1	150	100	5	Full factorial
− + −	1	150	300	2.5	Full factorial
− + +	1	150	300	5	Full factorial
+ − −	1	500	100	2.5	Full factorial
+ − +	1	500	100	5	Full factorial
+ + −	1	500	300	2.5	Full factorial
+ + +	1	500	300	5	Full factorial
–00	1	58	200	3.75	Axial
+00	1	592	200	3.75	Axial
0–0	1	325	48	3.75	Axial
0+0	1	325	352	3.75	Axial
00–	1	325	200	2	Axial
00+	1	325	200	5.7	Axial
000	1	325	200	3.75	Center axial
000	1	325	200	3.75	Center axial
000	1	325	200	3.75	Center axial
000	1	325	200	3.75	Center axial
000	1	325	200	3.75	Center axial
000	1	325	200	3.75	Center axial

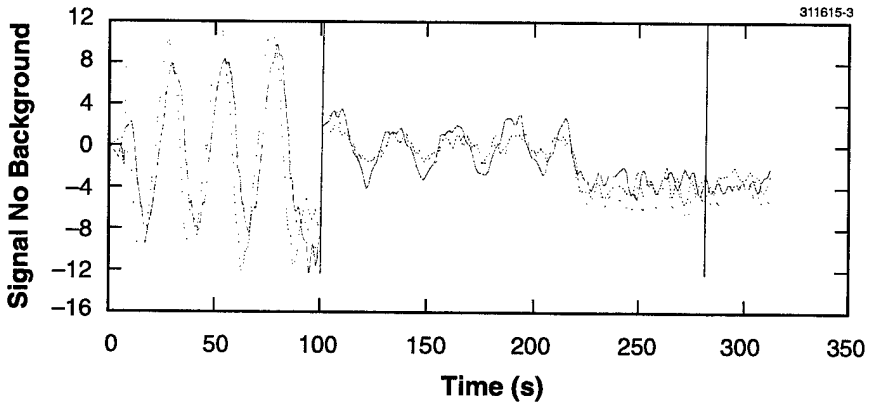


Figure 3-2. Representative trace from the imaging interferometric end point system of etched trilayer. The steps in the trace correspond to removal of the UV-4 imaging layer, removal of the photoresist in the fields (identified as end point), and the overetch. The resist index was set to 1.6 for these calculations. Patterned trilayer wafers were etched to completion plus a 50% overetch.

no doubt related to the large overetch time of 50%. These are seen in the various etched profiles and provide anecdotal evidence of the relation between chemical and physical etching effects for the various recipes used in the SDE.

The axial points of the design provided insight into the significance of the various plasma parameters. The selected images in Figures 3-3–3-5 illustrate the salient findings from the SDE. Each group of figures shows (a) etched sidewall roughness and (b) cross sections of isolated lines. Figure 3-3 demonstrates the effect of varying the TCP source power at 200-W chuck bias and 3.75 mTorr. Figure 3-4 shows the impact of varying the chuck bias at 325-W source power and 3.75 mTorr. Figure 3-5 shows the effects of varying the pressure at 325-W source power and 200-W chuck bias. Trends in the data, deduced from the SDE effects analysis and summarized in Table 3-2, lead us to draw a number of conclusions. The etch rate, which increases with both source power and chuck bias, is primarily driven by the source power with a smaller dependence on the chuck bias. The selectivity is controlled mainly by the chuck bias. Lateral etch decreases with increasing chuck bias but also depends on the magnitude of the source power. Uniformity increases with pressure and decreases with chuck bias, but has a parabolic dependence on source power.

Although sidewall roughness has not been quantified, qualitative evaluations can be made from the high-resolution SEM data. At conditions where there is undercutting of the profile, the sidewall is noticeably cleaner, although a sponge-like deformation of the polymer and the formation of columnar structures perpendicular to the substrate surface are observed. At other conditions a ridge-like deposition is observed on the sidewall. This is attributed to the forward sputtering and back scattering of the mask onto the sidewall [5]. This deposition is worse at low pressures and high chuck bias power, although it also increases with decreasing TCP source power, i.e., when there is a lower plasma density of reactive species, a longer

TABLE 3-2
Summary of Trends in Data from Statistical Design of Experiment Effects Analysis

Process Parameter	Transformer-Coupled Plasma Source Power Increase	Chuck Power Increase	Pressure Increase
Sidewall roughness	Strongly decreasing	Strongly increasing	Strongly decreasing
Profile anisotropy	See note*	Strongly increasing	Decreasing
Etch rate	Strongly increasing	Increasing	Weakly increasing
Selectivity	See note*	Strongly decreasing	Weakly increasing

*Depends on the magnitude of source power to chuck power, i.e., source power > chuck power, or source power < chuck power.

ion mean free path, and a higher ion energy or perhaps a relatively higher proportion of ions. In this case, the system is behaving more like a conventional RIE. In addition, examination of the resist sidewall polymer presents evidence of variation in the columnar structures (size, number of pillars, distribution) as well as a change in the background sponge-like morphology. The resist could be reticulated by long exposure to the plasma and the high energy density deposited in the sidewall, especially at high chuck bias. It is well known that there is surface heating of a thin layer during RIE [5]–[7]. It appears that a small amount of lateral etching to renew the surface is needed to minimize the sidewall roughness. However, too much lateral etching will reduce the critical dimension (CD). This can be folded into the design criteria for the dry development of TSI resist, where a certain amount of mask erosion and reduction of the CD from its original aerial image size already occurs. For source power > chuck bias and/or at higher pressure (4–5 mTorr), there appears to always be some lateral etch component. The chuck bias controls the anisotropy, but too much ion energy results in reduction of selectivity, copious mask redeposition on the sidewall, and "pillarization" of the resist. Long exposure to the plasma without lateral etch results in severe reticulation of the resist sidewall. The optimal etch conditions to reduce sidewall roughness, but maintain a vertical profile, point to source power > chuck bias, and moderately low pressure. The etch rate should be high to reduce the exposure time in the plasma. The temperature should be low to inhibit lateral etching.

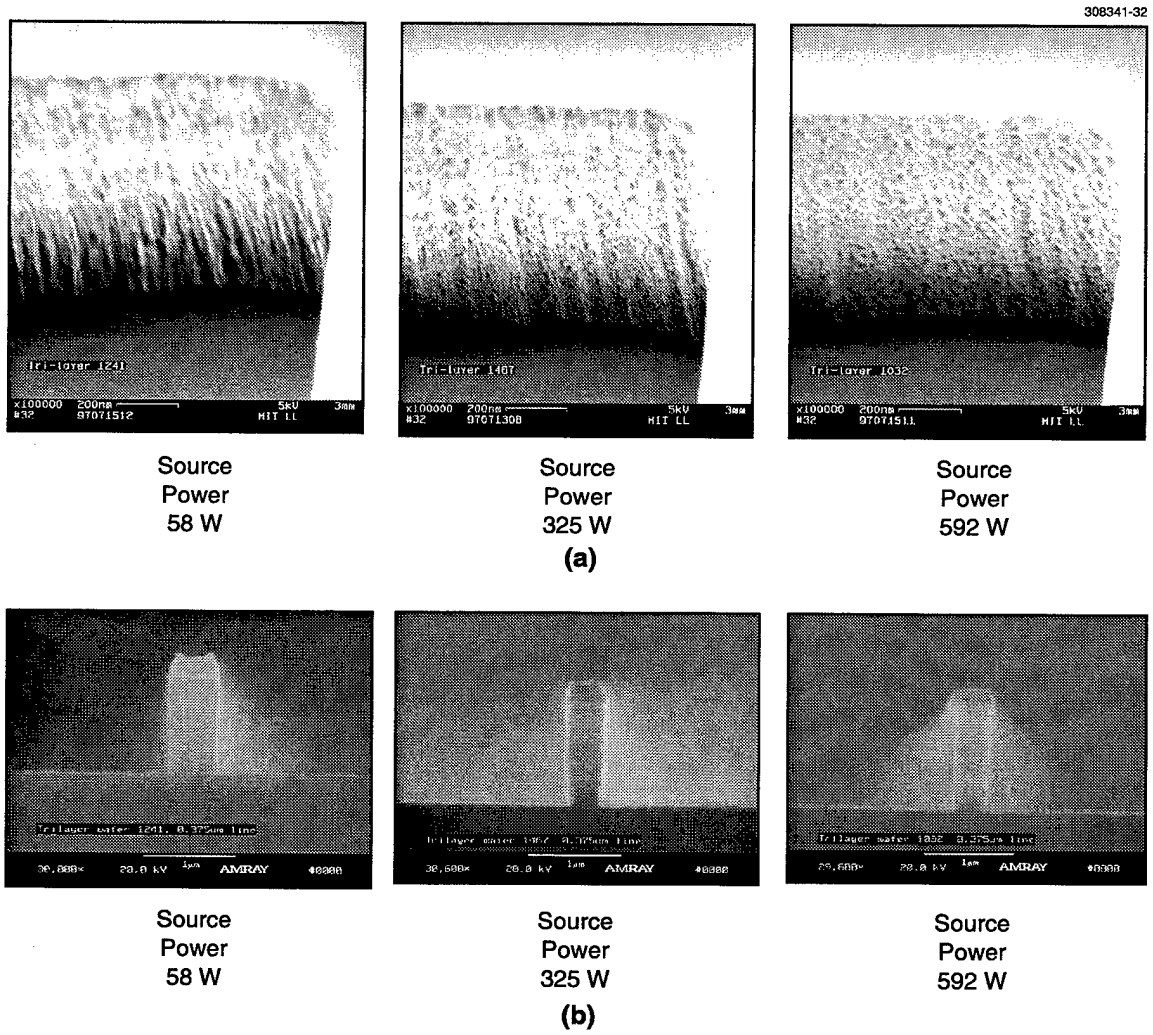
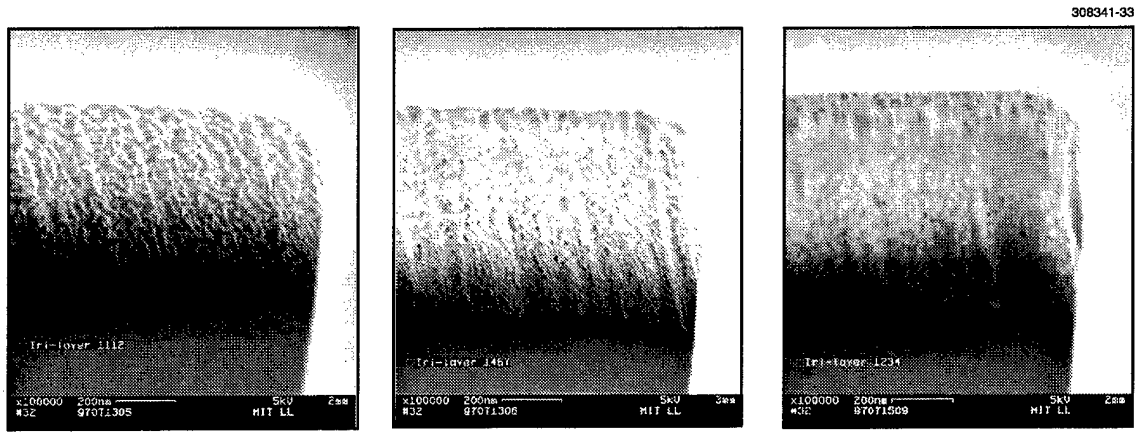
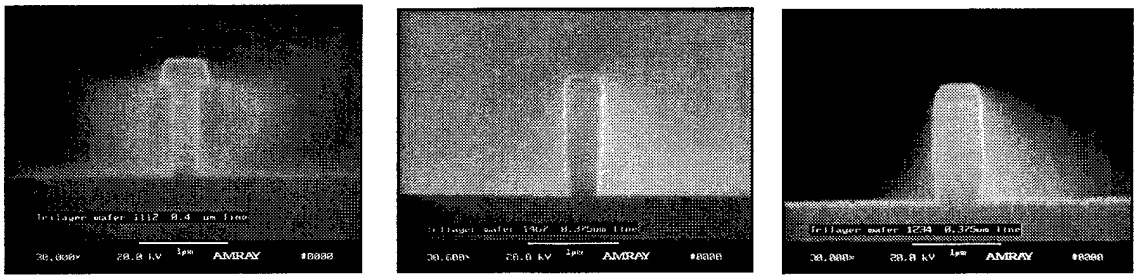


Figure 3-3. Scanning electron micrographs (SEMs) of (a) etched sidewall roughness and (b) cross sections of isolated lines for different TCP source power levels at 200-W chuck bias and 3.75 mTorr .



Chuck Power 48 W | Chuck Power 200 W | Chuck Power 352 W

(a)



Chuck Power 48 W | Chuck Power 200 W | Chuck Power 352 W

(b)

Figure 3-4. SEMs of (a) etched sidewall roughness and (b) cross sections of isolated lines for different chuck bias power levels at 325-W source power and 3.75 mTorr.

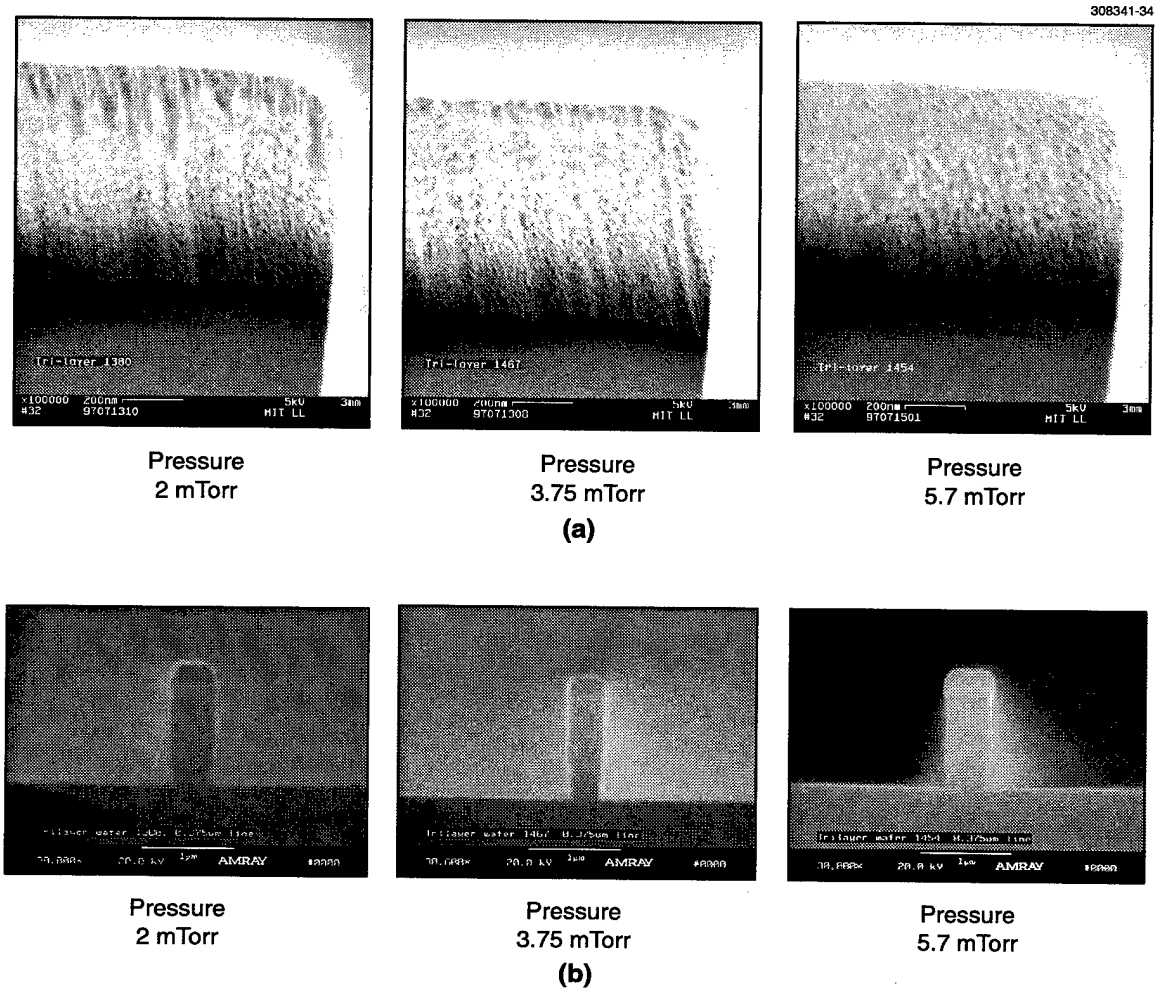


Figure 3-5. SEMs of (a) etched sidewall roughness and (b) cross sections of isolated lines for different pressure levels at 325-W source power and 200-W chuck bias.

In general, operating regimes can be divided into three groups: source power >> chuck power, source power ~ chuck power, and source power << chuck power. The TCP source power controls the electron density and hence the generation of active species. High source power results in a high etch rate, but when the chuck power is too low, even at –30°C, there is a large amount of lateral undercut. This is most clearly seen for 500-W TCP and 100-W chuck bias at 2.5 and 5 mTorr, and for 325-W TCP and 48-W chuck bias at 3.75 mTorr. This regime yields the least mask redeposition and sidewall roughness. At low TCP source power (58 W) the etch rate is low and the sidewall roughness increases with chuck power. Higher pressure, where there is increased scattering and lateral etching, lowers sidewall roughness. Selectivity is dominated by the chuck bias, decreasing as the bias power increases. The results obtained in these experiments have been used to empirically model the response surfaces (etch rates, uniformities, selectivities, profile, sidewall roughness). This is used to fit the observations to a general quadratic equation (the model) which relates the responses to the experimental variables (TCP source power, chuck bias power, and pressure) and interactions among them. A set of optimal etching parameters obtained by optimization of the response surfaces (the experimental model) has been used to identify a new set of baseline parameters, namely, a source power of 275 W and a chuck bias power of 250 W, at 5 mTorr pressure and –30°C.

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4. HIGH SPEED ELECTRONICS

4.1 ELASTIC-MEMBRANE MICROVALVES FOR MICROFLUIDIC NETWORK INTEGRATION

Microfluidics technologies are becoming important in the biochemical and biological processing fields because they offer advantages including low reagent consumption, highly parallel processing, and improved thermal management. Biochemical and biological processing protocols often make use of different flow and shear rates which have been difficult to control within a microfluidic manifold. Thus one of the critical keys to achieving microfluidic systems of useful complexity is the development of an integrated-microvalve technology. We have developed a new technique using elastic-membrane microvalves that can be implemented in large networks and that offers significant advantages over other valving methods. These integrated microvalves take advantage of two ideas to improve performance: flexible elastic membranes and three-dimensionally contoured valve geometries. The basic concept of our design is shown schematically in Figure 4-1. Pneumatic pressure applied to a flexible elastic membrane causes it to deform into the microfluidic flow path. As the membrane seals against the microchannel walls, hydrodynamic flow driven by the inlet pressure is shut off. Integrated valve seats and contoured sidewalls may be incorporated into the design to improve valve closure and flow characteristics.

Flexible elastic membranes give rise to some performance advantages, since elastic materials allow substantially larger deflections than the more classic materials used in semiconductor processing and silicon micromachining. Materials such as natural rubber (latex) allow large deflections before failure (e.g., a 25-μm-thick, 2.5-mm-diam latex membrane can deflect 2.5 mm at loads of less than 10 psi). Vieider et al. [1] and later Bousse et al. [2] have proposed microvalves based on the use of flexible materials; however,

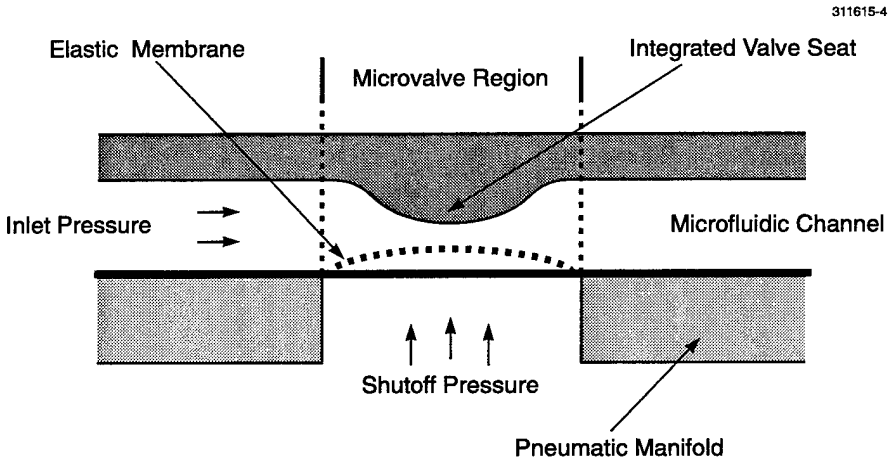

Figure 4-1. Schematic cross section of elastic-membrane microvalve. Pneumatic shutoff pressure causes elastic membrane to deform into the microfluidic channel. As the membrane seals against the integrated valve seat, hydrodynamic flow driven by the inlet pressure is turned off.

neither reported method takes full advantage of membrane elasticity. The type of load-deflection behavior exhibited by these highly deformable materials leads to some important consequences. First, flexible membranes allow better conformality over the valve seating surface. They therefore offer better sealing capability and are more robust to microfabrication imperfections. Valve dimensions can also be scaled down more effectively with such elastic membranes, since they can provide the deformation necessary to seal off flow in a much smaller footprint than that required by stiffer materials such as silicon or polyimide. This high level of integrability becomes an important consideration as microfluidic systems become more complex. As a corollary, small elastic valves will be able to shut off larger flows than their stiffer counterparts.

The microvalves reported here have other advantages that stem from the use of three-dimensional laser micromachining. Contoured geometries enabled by this sort of micromachining reduce both bubble formation during fluidic priming and cavitation during high-velocity flows. Microvalve structures presented by Lanzillotto et al. [3] demonstrate that this can indeed be a problem with more conventional valve designs, especially those with sharp edges. In addition, contoured geometries allow these valves to have much smaller dead volumes than competing designs to reduce the potential for contamination due to fluidic carryover. Finally, since the same processes used to fabricate microchannels are also used to fabricate microvalves, valves are easy to integrate into microfluidic systems. Electronic field stitching of three-dimensional laser-micromachined components enables rapid integrated-system design. Microreplication molding allows further low-cost duplication of these structures.

We use a laser microchemical etching process described previously by Bloomstein [4] to fabricate integrated valve seats for testing. The approach uses a fast chlorine-based laser-induced microchemical etching reaction and is computer-aided-design driven to achieve patterned plane-by-plane etching of the silicon substrate. The system used to perform this etching is shown in Figure 4-2. A silicon-wafer substrate is first mounted on a quartz stub within a chemical reaction chamber. A focused argon-ion laser beam is used to locally melt a portion of the silicon in the presence of chlorine gas. Volatile silicon chlorides are formed which rapidly diffuse from the surface, minimizing particulate formation. Through rapid deflection of the laser beam using computer-controlled X-Y galvanometers, etch depths per laser scan plane are typically limited to 1-μm shavings. A computer-controlled Z-stage is used to step and focus the X-Y laser scans in a plane-by-plane fashion. Substrate temperature can be elevated using an infrared source to improve reaction kinetics. Total removal rates range from 10^4 to 10^5 $\mu m^3/s$ for 1- to 10-μm lateral resolutions, respectively. Laser power is monitored by photodiode; etching progress is observed by charge-coupled device camera. Etched components can be field stitched together by mechanical translation of the substrate using the X-Y stage. Chemical activation reduces the energy requirement for removal, which in turn minimizes the damage potential relative to other patterning technologies that rely purely on thermal or mechanical energy (e.g., laser ablation, electrodischarge machining, and diamond turning). In order to further demonstrate manufacturability, etched structures have been replicated with submicron fidelity in transparent polymers using a molding process adapted from Whitesides [5]. Negative molds of the etched-silicon master are made by casting polydimethylsiloxane (PDMS) over the etched silicon surface, which has first been fluorinated with tridecafluoroctaltrichlorosilane (TDTS). A variety of polymers can then be cast over the negative mold to replicate a positive image which retains the etched configuration

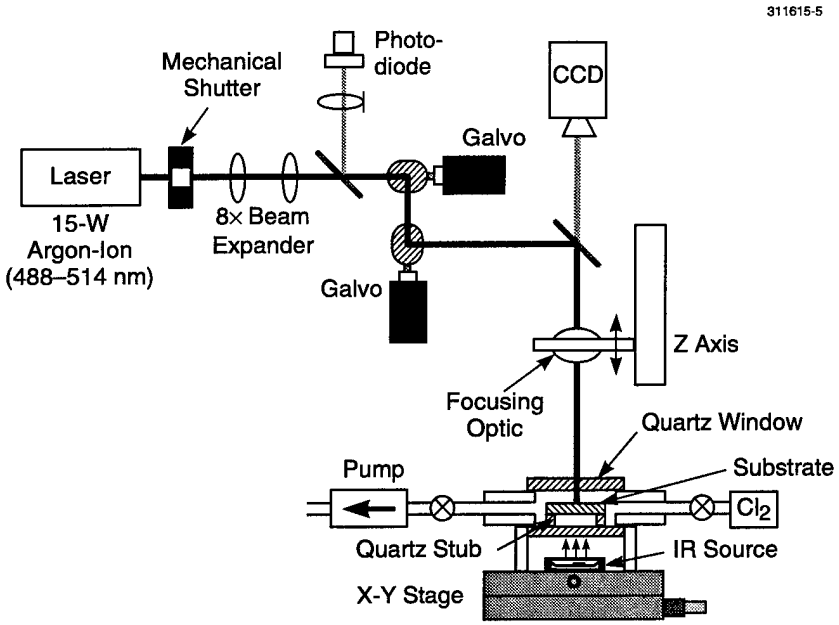

Figure 4-2. Schematic of system used to perform laser microchemical etching. Laser light from an argon-ion laser is scanned rapidly in the X and Y directions by two computer-controlled galvanometer mirrors, resulting in the removal of 1-μm shavings of silicon in the form of volatile silicon chlorides. A computer-controlled Z-stage is used to focus the laser scans in a plane-by-plane fashion. A reaction chamber holds the silicon substrate on a quartz stub and allows for the introduction of chlorine gas. Etching is monitored using a photodiode and CCD imaging. Substrate temperature can be elevated using an infrared source. Etched components can be field stitched together by mechanical translation of the substrate using the X-Y stage.

of the laser-etched silicon master. Since these polymers are optically transparent, visualization of fluidics is possible within the microchannels. Other replication techniques such as injection molding may also be used to improve manufacturability of these types of structures.

Several different valve-seat structures have been tested for microvalving performance. All structures had similar micromachined fluidic input/output connections to macromachined ports removed away from the valve region under test. Nominal channel length from input to output was 8 mm. In the peripheral areas away from the valve region, channel widths were 750 μm and channel depths were 100 μm. Three different silicon valve-seat designs were tested and labeled as unmodified, constricted, and expanded to reflect the relationship of the valve-seat area to the peripheral channels. The unmodified design maintained the nominal channel dimensions described above within the valve region and used the actual channel walls to form the valve seat. The micromachined saddle shape used as a valve seat in constricted designs had a minimum width at the silicon surface of 250 μm and a minimum depth at the center of the channel of 33 μm, as shown in Figure 4-3(a). The bowl shape used as a valve seat in expanded designs had a diameter of 1 mm and depth of 200 μm, as shown in Figure 4-3(b). All silicon-micromachined channels and valve seats were

fabricated maintaining a sinusoidal cross section perpendicular to the direction of flow to facilitate shutoff under membrane deflection. In addition to these silicon-micromachined parts, a macromachined plexiglas channel with rectangular cross section (vertical sidewalls) was fabricated to serve as a reference. Membranes were made of natural rubber and were nominally of 1.5-mm diameter and 25-μm thickness.

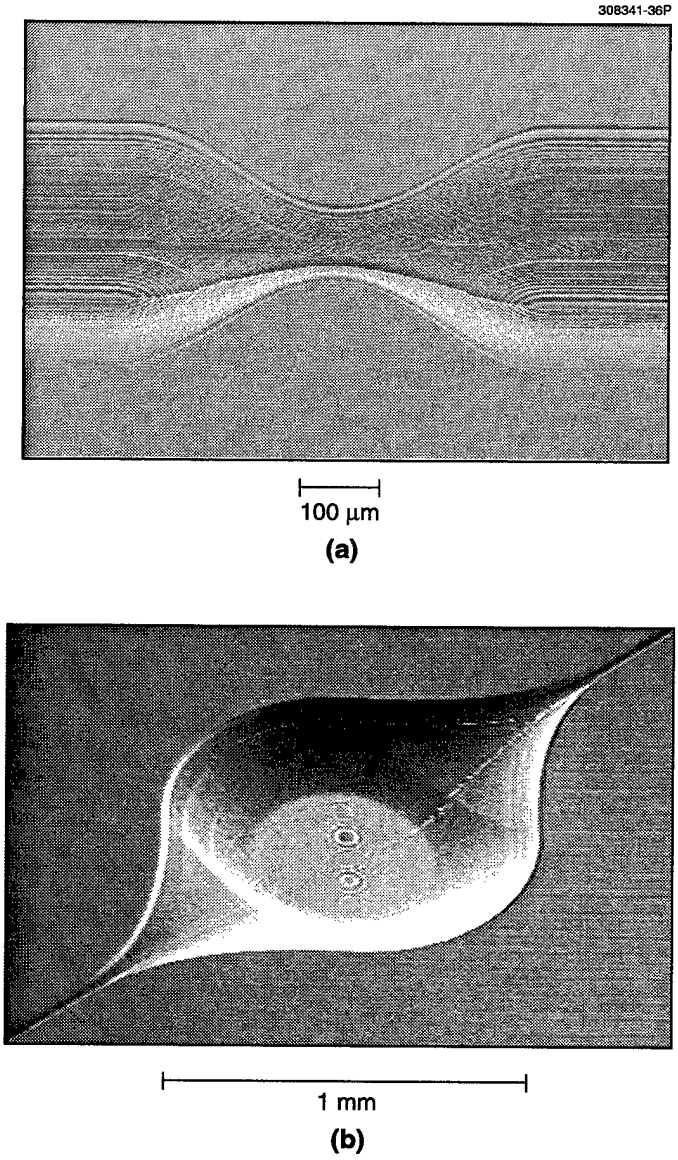

Figure 4-3. Laser-micromachined valve-seat geometries. (a) Micromachined constriction exhibiting saddle shape. Minimum width at the top silicon surface is 250 µm. Minimum depth at the center of the channel is 33 µm. (b) Micromachined expansion exhibiting bowl shape. Diameter at top surface is 1 mm. Maximum depth is 200 µm.

These test structures were assembled into testing manifolds as shown schematically in Figure 4-4. After micromachined parts were compression sealed to the underlying rubber, no leaks were observed. Fluid was delivered to and from the device using polyethyletherketone (PEEK) tubing which was compression fitted to attachment ports in a macromachined plexiglas manifold and further sealed with epoxy. Regulated compressed-air pressure was delivered to a holding reservoir to drive fluid hydrodynamically through the structure under test. A separate regulator was used to deliver pneumatic pressure to deflect the elastic membrane. Valve and reservoir fluid heights were adjusted to remove hydrodynamic loading effects due to gravity.

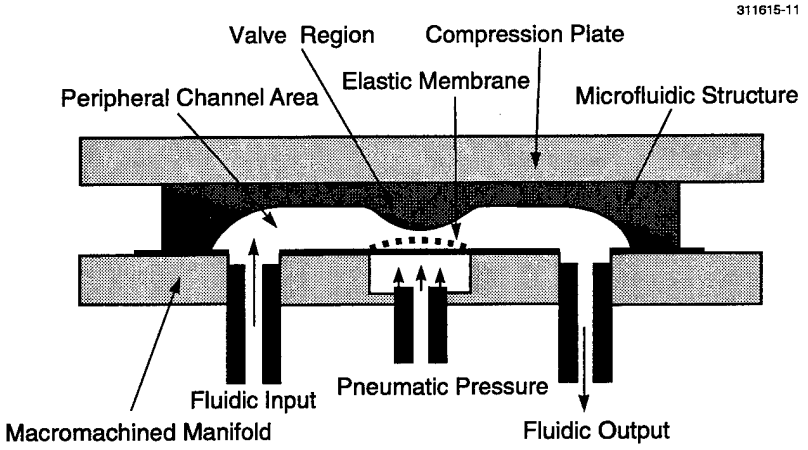

Figure 4-4. Cross section of valve-testing manifold.

Shutoff pressure, defined as the pressure required to reduce the flow rate to below 1% of the unperturbed value, was measured as a function of hydrodynamic inlet pressure. Similar valve shutoff results were obtained for the three silicon-micromachined structures with contoured edges. A distinct curve was obtained for the macromachined plexiglas channel. Results from the two most extreme cases, constricted silicon channel and rectangular plexiglas channel, are plotted in Figure 4-5. These curves are both linear, have a slope near unity, and in fact noticeably differ only by a small shift in Y-intercept. A pneumatic pressure only slightly greater than inlet pressure can be used to drive the valve into shutoff, which is a useful feature since both the pneumatics and hydraulics of a portable field unit could then be operated from a common regulated pressure source. The channel geometry has little effect on microvalve performance, except in the rectangular plexiglas-channel case where sidewall geometries are nearly vertical. In this vertical-sidewall case, when pneumatic pressure is just larger than inlet pressure, leakage paths are still found at the channel sidewalls. The elastic membrane requires additional pressure to fully conform to the sidewalls of the channel, leading to a corresponding shift in Y-intercept. However, the fact that this flow can be shut off at all is a dramatic demonstration of the flexibility of the elastic membrane, and cannot be achieved

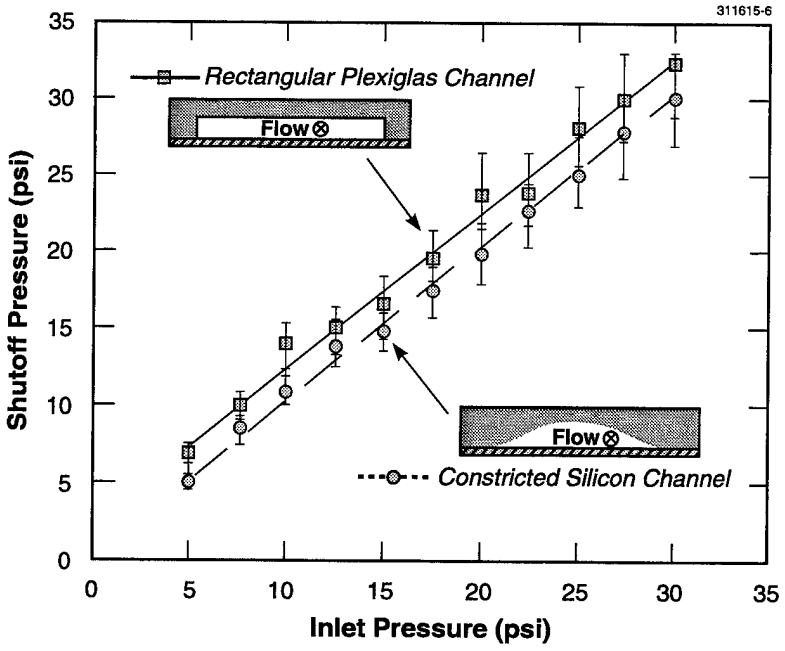

Figure 4-5. Microvalve test data from constricted silicon-channel and rectangular plexiglas-channel geometries. Note near-unity slope and near-zero Y-intercept.

by the stiffer materials used in conventional micromachining. Thus, the contouring of our microvalves gives rise to performance advantages in fluidic priming, high-velocity flows, and dead-volume reduction, while the behavior of the highly flexible membrane dominates the shutoff properties of these valves.

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5. MICROELECTRONICS

5.1 LOW-LIGHT-LEVEL 640 × 480-PIXEL CCD CAMERA FOR NIGHT VISION APPLICATIONS

A 640 × 480-pixel charge-coupled device (CCD) imager and camera electronics have been developed for night vision imaging. The CCD camera, operating at 30 frames per second (fps), has demonstrated good performance below starlight illumination conditions. This report describes the performance and features of the CCD imager and camera electronics.

Figure 5-1 shows a schematic and photograph of the 640 × 480-pixel CCD imager. The imager has a split frame-transfer architecture with two frame-store arrays located on opposite sides of the imaging array. The CCD has eight serial registers with four registers adjacent to each frame store. Each output register has a two-stage readout amplifier that is responsible for the output of a 160 × 240-pixel section of the 640 × 480-pixel image. The multiple ports reduce the pixel frequency per port, for a given frame rate, thereby reducing readout noise. Back illumination of the imager [1] results in near-reflection-limited quantum efficiency in the visible (400–700 nm) and good response in the near infrared (700–900 nm). An antiblooming drain [2] design inhibits column blooming for signal levels up to at least 10^5 times pixel full well. Figure 5-2 shows the CCD imager mounted on a two-stage TE-cooler inside a 68-pin package. The internal cooler

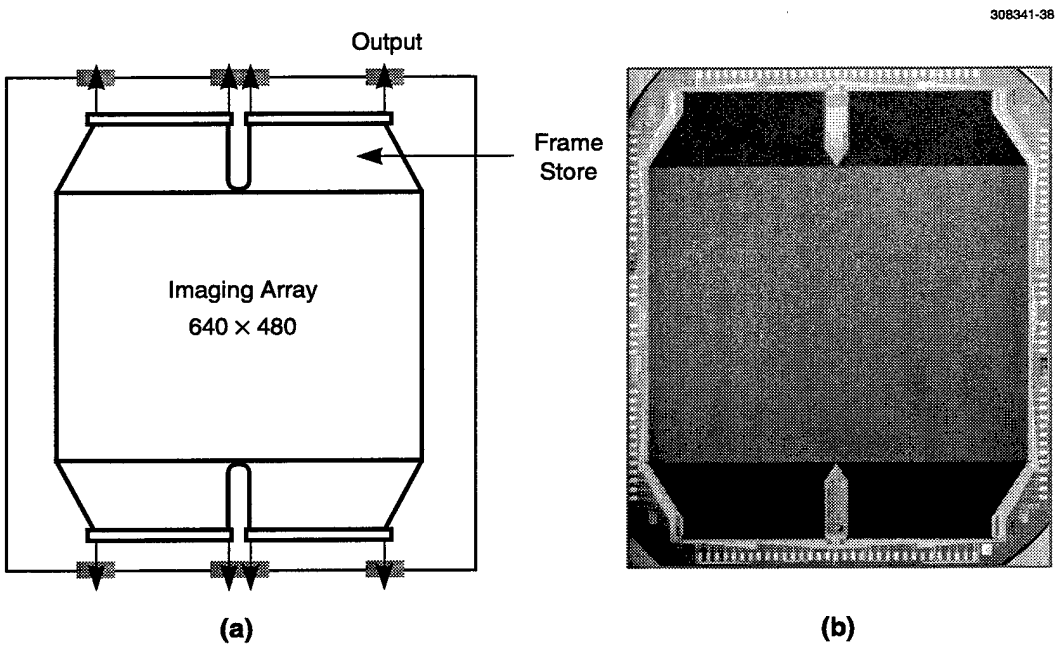

Figure 5-1. (a) Schematic and (b) photograph of a 640 × 480-pixel CCD imager.

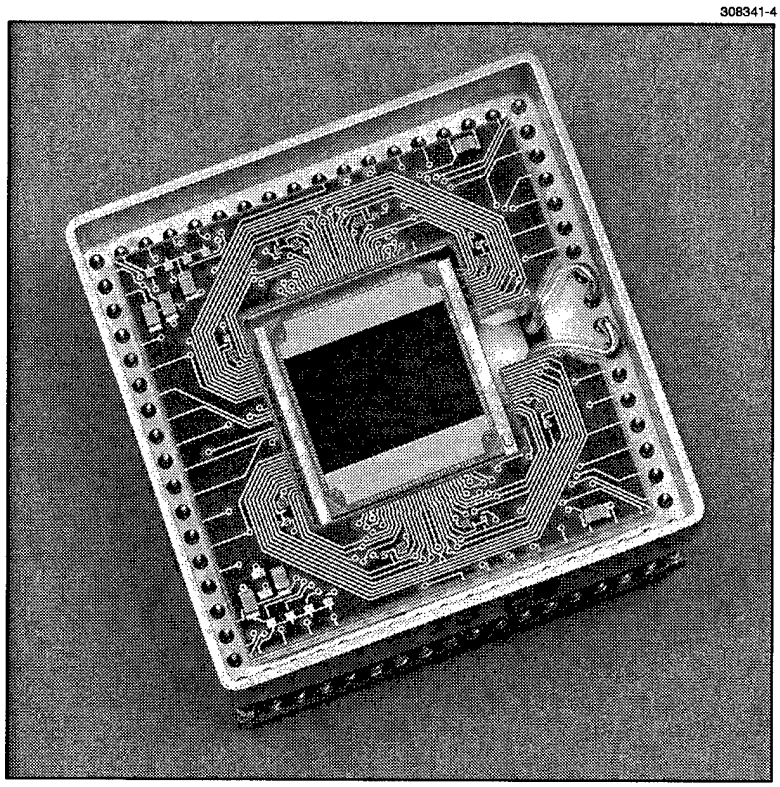

Figure 5-2. Photograph of the 68-pin package with internal TE-cooler.

lowers the CCD temperature to –35°C where the package tub, used for the heat sink, is held at 25°C. The cooling reduces the dark current background and noise to negligible levels at the 30-fps operation.

The CCD camera electronics, which operates the CCD imager at variable frame rates, has a 12-bit dynamic range. The camera electronics consists of three multilayer printed circuit boards. The board set provides all the digital timing and analog drive and post-processing circuitry necessary to operate the CCD. The board that contains the CCD also has eight analog output chains, one for each CCD readout amplifier. When the camera is operated at 30 fps, the pixel rate per port is 1.33 MHz and the readout noise at this frequency is 4 e^- rms. The camera has two imaging modes, full frame (640 × 480 pixels) or binned (320 × 240 pixels), where the binned mode is used to improve resolution at low light levels.

In a laboratory environment, the CCD camera has demonstrated sensitivity below starlight illuminance conditions. Figure 5-3 shows contrast resolution chart images for illumination conditions ranging from full moon (33.3 mLux) to half starlight (1.0 mLux). The camera was operated at 30 fps in the full frame mode. The three resolution contrast charts shown for different lighting conditions have contrasts of

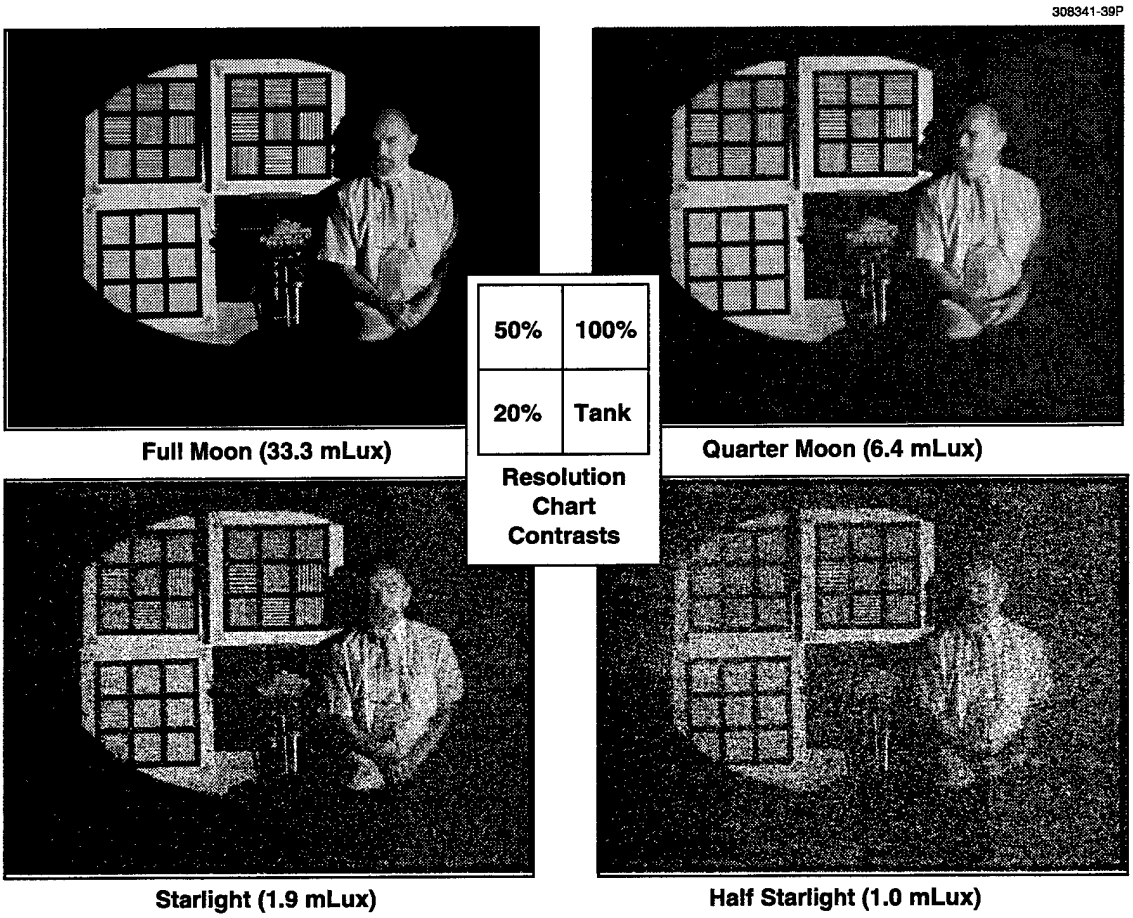

Figure 5-3. Constrast resolution chart images from the 640 × 480-pixel CCD camera for lighting conditions ranging from full moon to half starlight. The camera is operating at 30 frames per second and the lens used in obtaining the images had an f-number of 1.4.

20, 50, and 100%. The bar pattern frequency in each resolution chart has line pairs per millimeter (lp/mm) down to the CCD Nyquist limit (~21 lp/mm). Even under starlight conditions, the 20% contrast bar patterns with 21 lp/mm were visible. The CCD camera has been used in nighttime driving experiments (van driven without headlights) under natural lighting conditions where the scene illumination was measured at a few millilux (near starlight illumination).

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6. ANALOG DEVICE TECHNOLOGY

6.1 MODEL OF RESISTOR FABRICATION IN A LOW-TEMPERATURE SUPERCONDUCTIVE ELECTRONICS PROCESS

The operation of low-temperature, Josephson junction-based, superconductive monolithic circuits at clock speeds approaching 50 GHz for mixed-signal applications will require precise control of critical parameters of the circuit elements. We report here on recent progress in understanding phenomena that occur in the resistor fabrication process and that cause previously unexplained variations in resistor values. This new understanding will help us to improve the fabrication yield and precision of resistors used in Josephson junction circuits.

The Lincoln Laboratory low-temperature (4.2 K) superconductive electronics process is based on a doubly planarized all-refractory superconducting technology (DPARTS) [1]. The junctions are formed in a $Nb/AlO_x/Nb$ trilayer, the wiring and inductors are made of niobium, and the resistors are fashioned from a Pt film using a thinner Ti layer to promote adhesion of the Pt to the SiO_2 substrate. Typical resistors have a sheet resistance R_s of ~0.6 Ω/sq, with a 3σ spread of ±15%. This value of the sheet resistance is three orders of magnitude larger than one would estimate based on the resistivity of pure bulk platinum at 4.2 K. The observed value for the low-temperature resistivity is most likely dominated by scattering of conduction electrons by impurities, grain boundaries, and the film surface—factors which are strongly process-dependent.

Post-process, low-temperature testing of a closely spaced array of resistors of varying widths revealed an unexpected anomaly in the measured resistance values. The conductance G of an ideal resistor of width w, length L, thickness d, and isotropic resistivity ρ is given by

$$G = \frac{wd}{L\rho} \ . \tag{6.1}$$

According to this equation, a plot of G vs nominal width should be a line through the origin. Figure 6-1(a) shows that the empirical relationship is more closely fit by the relation

$$G = \frac{(w - w_o)d}{L\rho} \ , \tag{6.2}$$

where w_o ~ 1.5 μm is the w intercept and is due to a resistor sizing error, or "electrical" undercut. We term this effect electrical because, when measured under optical and electron microscopes, these resistors have widths within ~0.1 μm of their nominal values. As we show below, this electrical undercut can result from nonuniform resistivity along the cross section of the resistor. We have observed that the measured value of w_o varies from run to run with a mean value of ~1.75 μm and a standard deviation of ~10%—too large for use in high-performance circuits.

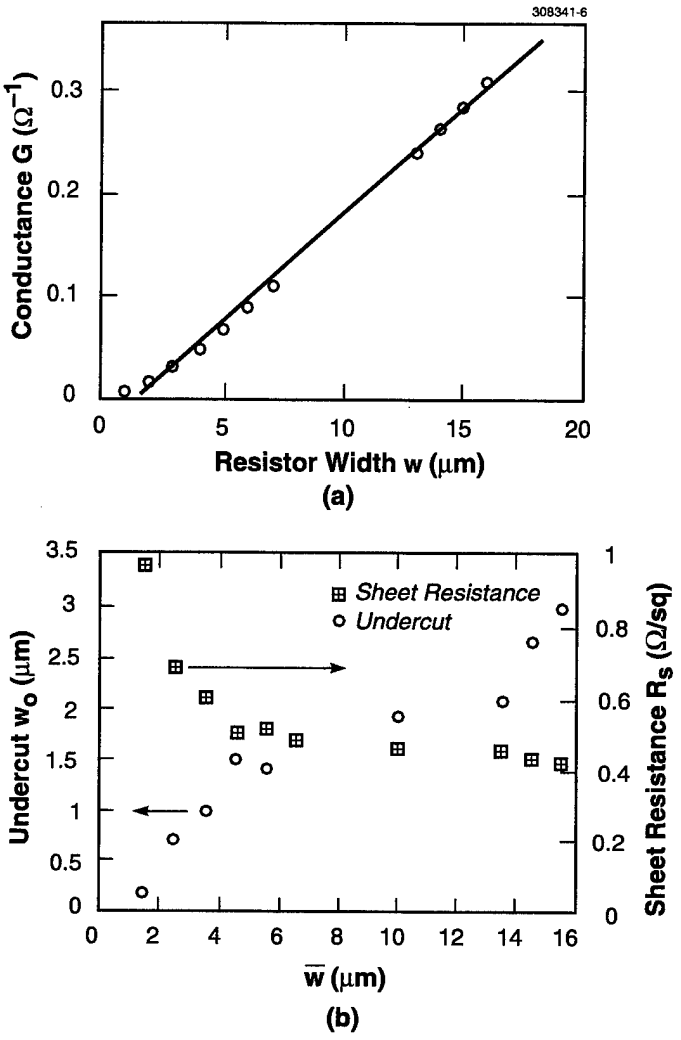

Figure 6-1. (a) Conductance vs nominal resistor width for a variety of resistors at low temperature, showing the resistor sizing error w_o (the w-intercept value). The slope of this curve is inversely proportional to the sheet resistance R_s. (b) w_o and R_s as a function of $\bar{w}$, obtained by fitting Equation (6.2) to data of two adjacent points ($\bar{w}$ is the average resistor width of the two data points). This shows that narrower resistors have a larger sheet resistance and a smaller sizing error.

To establish which process variables were relevant to the observed variation in resistor undercut, we first undertook a more detailed examination of the G vs w data and observed an interesting systematic deviation from the linear empirical relationship given above. By fitting Equation (6.2) to adjacent data points, one can extract the value of the undercut w_o and effective sheet resistance $R_s = \rho/d$ as a function of $\overline{w}$, where $\overline{w}$ is taken to be the average of the w of the adjacent data points. If the empirical relationship given in (6.2) were accurate, there would be no observable trend to these data. Figure 6-1(b) shows instead that the undercut decreases monotonically with decreasing $\overline{w}$, while the sheet resistance increases with decreasing $\overline{w}$.

The origin of both the undercut w_o and the variation of w_o and R_s with $\overline{w}$ can be explained by examining the details of the resistor fabrication process. The resistors were formed on a planarized SiO_2 substrate using a liftoff process. The substrate was first coated with a patterned layer of photoresist, then covered with an evaporated 100-Å-Ti/900-Å-Pt metal layer. The photoresist was removed by immersion in an acetone bath, leaving behind resistor metal where the substrate had been exposed to the evaporation. The resistors were placed so as not to cross any underlying circuit topography. To explain the observed sizing error in the resistors, we hypothesize that impurities are unevenly distributed across the film as a result of outgassing of contaminants from the resist sidewalls during the evaporation process. Figure 6-2 shows the microscopic picture of the resist definition process, during which a fraction of the impurity atoms that desorb from the resist surface are incorporated into the platinum film. Such a process would be expected to produce the effects observed, including an effective undercut whose magnitude would be on the order of the resist thickness, ~1.5 μm.

The model that we developed to calculate the effect of outgassing assumed that the resistivity consisted of two contributions: the first due to surface scattering, grain boundary scattering, and baseline impurities incorporated in the film from the vacuum system and the source, and the second due to impurities incorporated into the film from the resist sidewall outgassing. The first contribution is uniformly distributed and so should be the same for patterned and unpatterned wafers; it was determined by measuring the sheet resistance of unpatterned regions of the wafer both at room temperature and at 4.2 K. The result of this measurement was used as an input parameter to the calculation. The second contribution was calculated by assuming that the resistivity due to impurities was linearly proportional to the impurity concentration (Nordheim's rule). The rates of outgassing and of incorporation of impurities into the metal film were combined with the scattering cross section of conduction electrons with impurity atoms into a single, multiplicative fitting parameter.

We assumed that the outgassing was isotropic and that the rate did not vary along the resist profile. The resulting analytic expression for R_s as a function of position x across the width of the resistor is

$$R_s(x) = \kappa\left\{\log\left[\left(\frac{x^2+D^2}{x^2}\right)\times\left(\frac{(x-w)^2+D^2}{(x-w)^2}\right)\right]\right\} + R_o \quad , \tag{6.3}$$

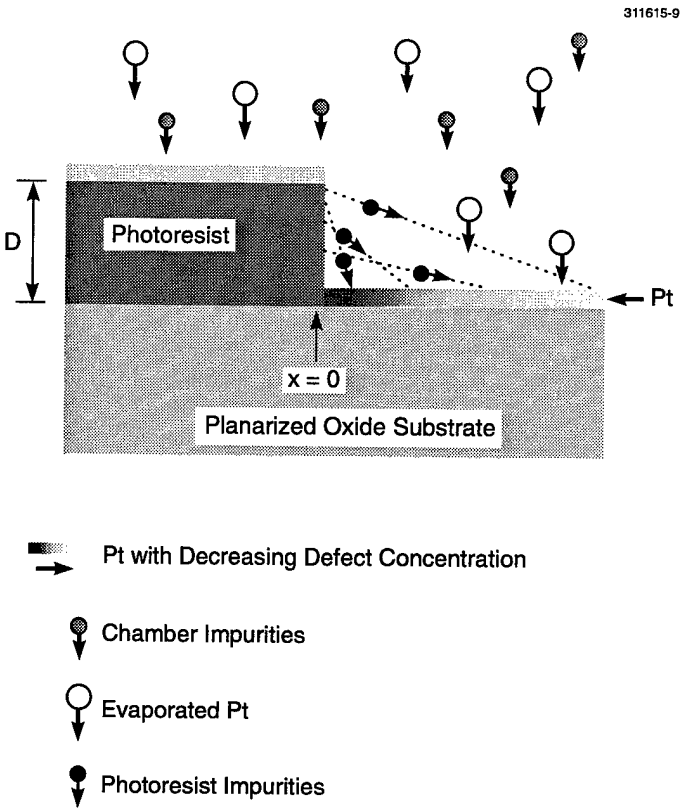

Figure 6-2. Microscopic illustration of the deposition process for the resistors as hypothesized to explain the resistor sizing error. Contaminants desorb from the resist sidewalls. These contaminants are incorporated into the resistors primarily near the edges, creating a region of high resistivity, and leading to an electrical undercut.

where D is the thickness of the resist, κ is the multiplicative fitting constant, and R_o is a constant term resulting from background impurities in the vacuum system. Figure 6-3 shows the calculated $R_s(x)$ profiles for two resistor widths.

The conductance was then obtained by numerically integrating $1/R_s(x)$ across the width of the resistor. Figure 6-4 shows a comparison between theoretical conductance values and the data from Figure 6-1. Notice the improvement of the fit relative to the simple linear theory, even though this is only a single-parameter fit, while the empirical model given in Equation (6.2) is a two-parameter fit. This model predicts correctly that narrower resistors should have higher sheet resistance and lower undercut.

Additional experiments where processing parameters such as resist thickness and bake conditions are varied might further validate the theory presented. Our hypothesis also suggests several paths for eliminating the undercut effect: First, it is advisable to use a material where the resistivity due to undesired

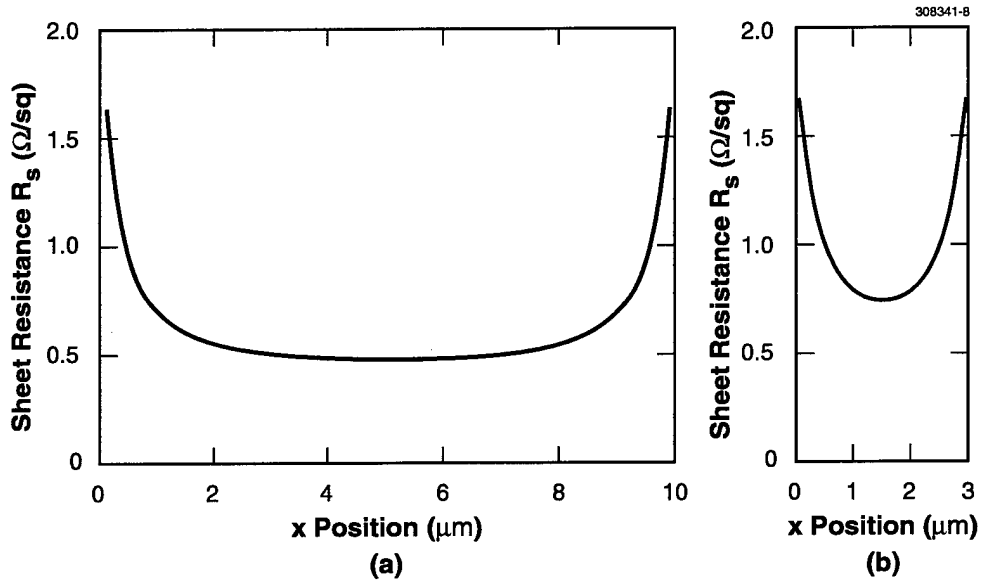

Figure 6-3. Calculated sheet resistance vs position across a resistor for (a) 10-μm-wide resistors and (b) 3-μm-wide resistors. The sheet resistance diverges at the resist. The narrower resistors have a higher mean sheet resistance because the contamination from the edge extends into a larger fraction of the resistor; correspondingly, the resistor sizing error appears to be smaller.

impurities is small relative to the baseline resistivity. IBM successfully pioneered the use of PtRh as a resistor material [2], and we have completed experiments that establish that PtRh resistors do not exhibit a measurable electrical undercut effect. Second, patterning by etching is preferable to patterning by liftoff. Unfortunately, platinum etching is not easily accomplished; it can result in severe etch residue, or "fencing" removal difficulties, and leads to problems with etch-chamber conditions.

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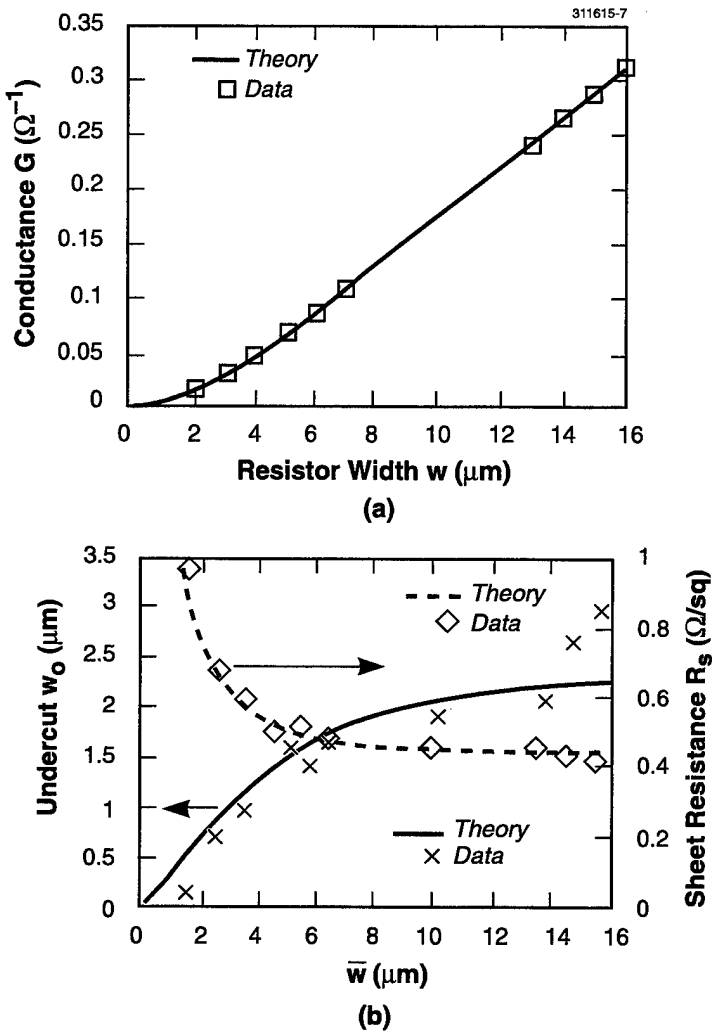

Figure 6-4. (a) Comparison of measured and calculated values for the conductance of resistors with varying widths. The single fitting parameter used for the theory was a combination of the outgassing rate from the resist sidewalls, the incorporation rate of impurities into the metal film, and the cross section of scattering between electrons and the impurity atoms. (b) Fit of the data given in Figure 6-1(b) to the theory, using the same fitting parameter as in (a).

7. ADVANCED SILICON TECHNOLOGY

7.1 THE SLOTFET AS A TRANSISTOR FOR THE 25-nm GENERATION

Transistors in today's most advanced commercially available integrated circuits, as well as the ones built at Lincoln Laboratory, have gate lengths of 0.25 μm, or 250 nm. This length is one of the most important parameters in determining the speed, and therefore the computational capability, of digital systems, and it has been shrinking steadily for decades. It will certainly continue to shrink for some years to come, but just how short the gates can become and still make transistors which behave conventionally and can be used in circuit architectures much like today's is not entirely clear. To explore this question, Lincoln Laboratory recently started a program to build nearly conventional metal-oxide-silicon field-effect transistors (MOSFETs) with gate length of 25 nm, ten times smaller than the advanced devices of today. At this dimension we believe that the device physics is almost unchanged from that of larger devices, while below 25 nm the quantum effects will become much more important.

While the basic physics may be unchanged, the practical problems of fabricating such a device are formidable. The status of our work on some of these problems is described here. The first efforts are focused on building a device called the SLOTFET, so named because the most critical feature, the gate, is formed on the inside of a narrow slot which was etched into a disposable material. This approach provides a gate length which is less than can be defined lithographically, the gate material does not need to be etched (which allows use of materials which are otherwise desirable), and the gate is self-aligned both to the source and drain and to the extremely thin region needed for the channel (which minimizes parasitic capacitance and resistance, and hence maximizes the transistor's speed).

The process begins with silicon-on-insulator (SOI) material thinned to about 50 nm and patterned to form a separate silicon island for each transistor, just as in the 0.25-μm program described previously [1]. It continues as illustrated in Figure 7-1. An oxide layer is deposited and polished to provide a flat surface for lithography. A slot is patterned and etched through this oxide and part way through the silicon. While 25-nm and even smaller slots could be written with an electron beam, today's e-beam lithography is extremely slow and is not practical for patterning large circuits. We are instead using optical lithography, as in nearly all integrated circuit manufacturing, but extending its capability through phase-shift masking. Using either Lincoln's unique 193-nm step-and-scan system or a more conventional 248-nm (deep uv) stepper we can define 100-nm, or even smaller, lines in photoresist. Examples are shown later in this report.

Silicon nitride is deposited conformally and then etched anisotropically to form spacers inside the slot. The exposed silicon is then oxidized, cleaned, and oxidized again to form the extremely thin (2–3 nm) gate dielectric, and the gate material is deposited and polished to form the gate. The gate material and its processing are described in detail below. The disposable oxide is removed, and from here on the process nearly duplicates the one for 0.25-μm devices.

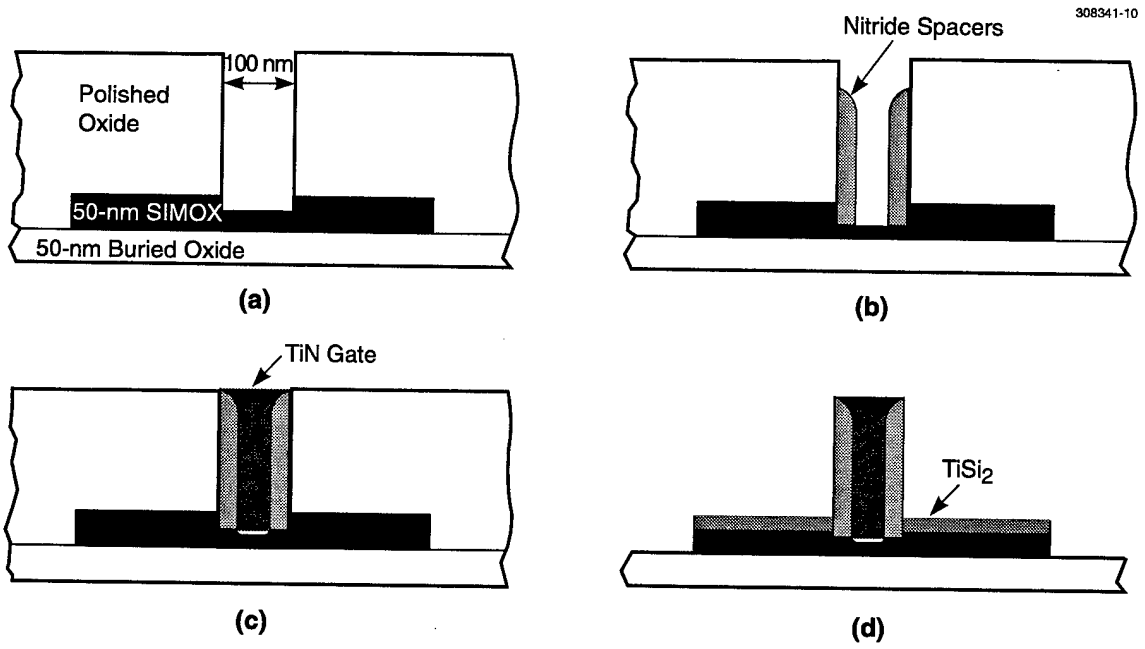

Figure 7-1. Summary of SLOTFET fabrication process: (a) Etch slot in disposable oxide, (b) form nitride spacers inside slot, (c) grow gate oxide (damascene formation of gate metal), and (d) dispose of oxide and form silicide. Before and after the steps indicated the process is very similar to standard 0.25-μm silicon-on-insulator (SOI) fabrication.

The similarity to standard processing is an important advantage of this approach, because it minimizes the new problems that need to be solved. The key difference between the SLOTFET and longer devices is the self-alignment between the gate and the thin silicon region. Simulations show that for good transistor behavior at 25-nm length the Si thickness in the active region must be only about 5 nm. Such a thin film, even if degenerately doped, has a sheet resistivity of about 2000 Ω/sq, so the length required for alignment tolerance would add enough resistance to severely degrade the current carried by the transistor.

This process and the resulting devices have been simulated using Athena and Atlas, respectively, two commercially available simulators from SILVACO International. The cross section of a transistor active region from Athena is illustrated in Figure 7-2. The geometry is as expected from the conceptual drawings of Figure 7-1, except for the small "ears" at the edges of the gate. These form because oxidation occurs under the nitride spacer, forcing it away from the silicon. Cleaning removes this oxide, and gate oxide growth does not completely fill the space between silicon and nitride. In a conformal deposition process, assumed in the simulation, this gap is filled by the gate material, forming the ear. Exactly what really happens in the bottom of the narrow slot will be determined experimentally.

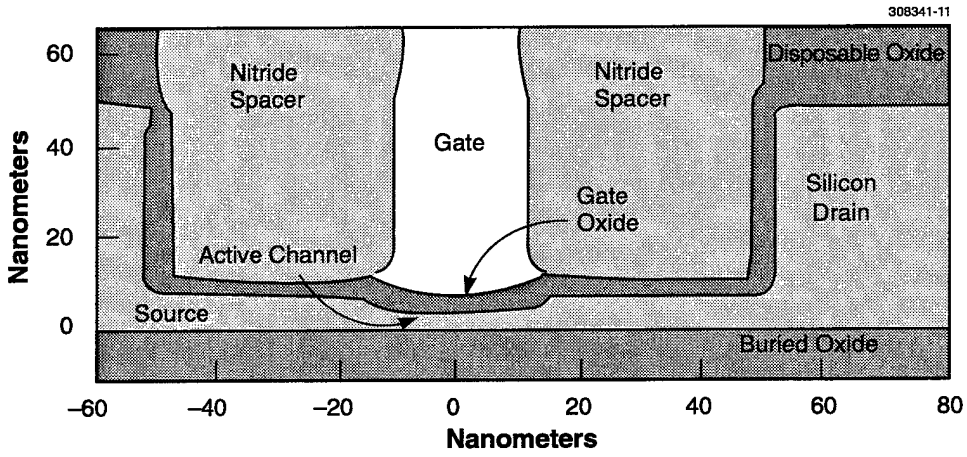

Figure 7-2. Cross section of a SLOTFET as simulated by Athena, after the gate is created and before the disposable oxide is removed. The active channel in this example is 5 nm thick and the gate oxide is 3 nm thick. The gap between the nitride spacers was 20 nm before any oxide was grown.

Typical current-voltage curves for such an *n*-channel device are shown in Figure 7-3, as simulated by Atlas, assuming the TiN gate discussed below. The drain characteristics look quite normal, with saturation transconductance at 1 V of 1070 μS/μm. Threshold voltage at V_{drain} = 1 V is 252 mV, and the threshold shift between V_{drain} = 50 mV and 1 V is about 80 mV, which are quite acceptable. These values are for silicon thickness of 5 nm and gate oxide of 3 nm. Making the silicon thin is extremely important. Increasing it to 10 nm has negligible effect on transconductance, but the 50-mV vs 1-V threshold shift increases to 190 mV, and the off-state leakage current increases by a factor of 100.

The large improvement by thinning the silicon occurs because the conductive layer is closer to the gate and hence more completely under its control. In contrast, reduction of gate oxide to 2 nm improves performance only modestly, probably because the inversion layer thickness is substantial on this scale, so the effective gate insulator is thicker than the actual oxide. (This simulation is strictly classical and ignores quantization in the inversion layer which would make the inversion layer thickness greater and hence would decrease the advantage of thinning the gate oxide.)

The slot used to define the SLOTFET gate is very narrow, 100 nm. This aggressive critical dimension (CD) can be patterned by chromeless phase-shift lithography using the 193- or 248-nm exposure tools available at Lincoln Laboratory. This method is ideal for printing small isolated lines and slots. We start with a standard chrome-on-quartz reticle and use the chrome as a mask to etch the quartz to a depth of $D = \lambda/2(n-1)$, where λ is the wavelength and n is the index of refraction of the quartz, corresponding to a 180° phase shift of the incident light. The chrome is then stripped off, leaving a quartz relief structure to be used for the phase-shift exposures. The light passing through the quartz on opposite sides of a step is out of

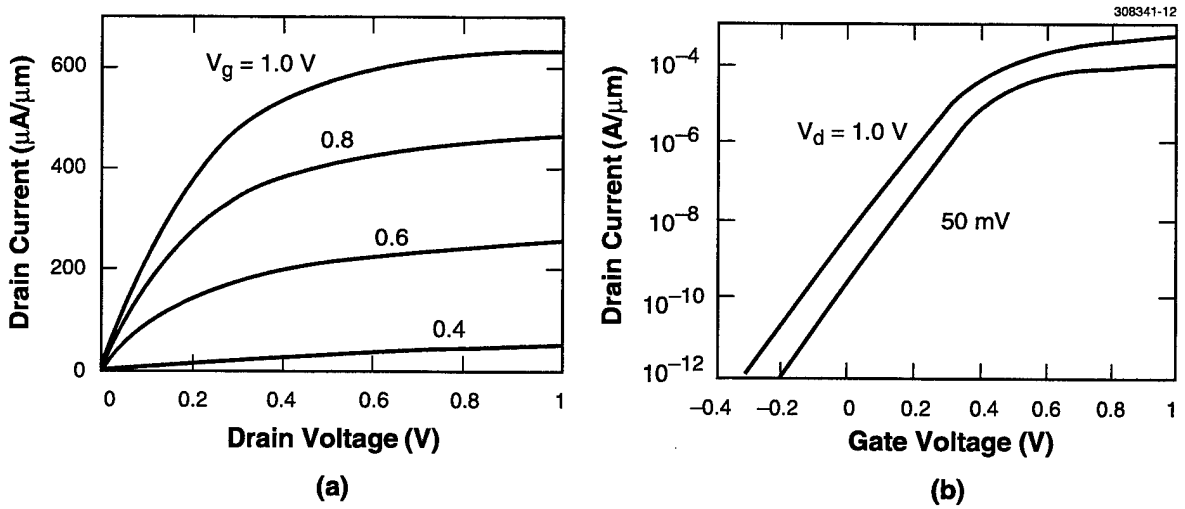

Figure 7-3. Drain current vs (a) drain voltage and (b) gate voltage from Atlas simulation of a SLOTFET with 25-nm channel length, 3-nm gate oxide, 5-nm silicon, and 50-nm buried oxide, with an n-type substrate.

phase by 180°, resulting in destructive interference which produces a narrow dark line in the aerial image. The dark line is transferred to photoresist as a line in positive resist or a slot in negative resist. The benefits of this method are linewidths much smaller (about 2×) than the incident wavelength owing to the small region of destructive interference, and a large depth of focus since destructive interference is independent of focus.

We have done a number of experiments on chromeless phase shifting using a variety of resists on both the 193- and 248-nm tools. Assistance with the proper mask design, the illumination parameters, and the resist thicknesses was provided by modeling using Optolith, another SILVACO tool. Although the smallest features in the aerial image should be produced by the 193-nm system, the narrowest features in photoresist have come from the 248-nm stepper. This result is mostly due to the relative maturity of the resists available for the two wavelengths. Furthermore, the SLOTFET requires a negative resist to pattern the slot, and no negative resist is yet commercially available for 193 nm.

Phase-shift patterning experiments to date have concentrated on defining narrow lines in positive resist, soon to be followed by slots in negative resist. It was found that the typical resist thickness of 700 nm resulted in such a high aspect ratio that the resist lines tended to be mechanically unstable, so much thinner resist was used. The wafer surface in the SLOTFET process is almost perfectly flat, and the selectivity of oxide or nitride etch rate to that of photoresist is high, so very little resist is needed. The best results so far used Shipley UV-5 resist diluted with solvent to make a 300-nm film. Figure 7-4 is a top-down scanning electron microscope view of a polycrystalline silicon (poly) line etched with a

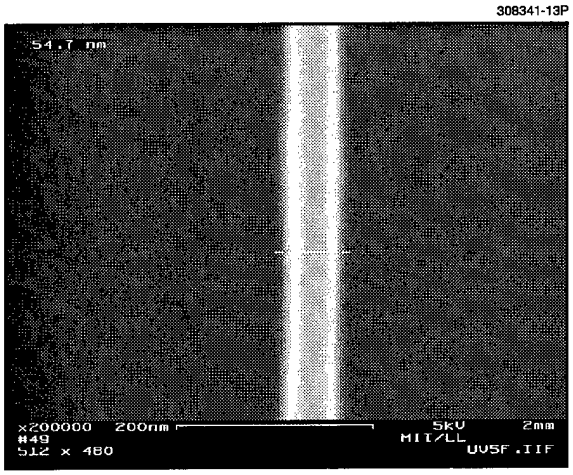

Figure 7-4. Part of 55-nm-wide, 30-μm-long polysilicon line patterned with phase-shift optical lithography and etched by high-density plasma. Such a feature could be used to make a conventional metal-oxide-silicon field-effect transistor (MOSFET) gate.

high-density plasma after phase-shift pattern definition using the 248-nm stepper. The line is 55 nm wide, with smooth edges, and is 30 μm long with uniform width along its length. It is expected that similar width slots will be produced in the future using negative resist.

The process window for printing small lines is just as important as the minimum CD achieved. Figure 7-5 illustrates the low degree of process sensitivity. The linewidth varies linearly with the exposure dose over a wide range with a relatively low slope of 170 nm/mJ, which corresponds to 10% change in CD for 8% change in dose at the nominal 100-nm linewidth. Furthermore, the linewidth is nearly independent of defocus over a wide range as a consequence of phase-shift exposure, which greatly diminishes one of the principal contributors to CD variation.

Threshold voltage control is one of the most critical components in determining the overall performance of a CMOS circuit. This problem is especially severe for fully depleted SOI CMOS technology, since the total silicon body depletion charge is directly related to the SOI thickness, which may be difficult to control [2]. In most cases, symmetrical thresholds for NMOS and PMOS are desirable. Conventional CMOS processing uses dopants to adjust the poly-Si gate workfunction and the Si body depletion charge for setting the threshold voltage. To achieve symmetrical thresholds and surface channel operation for optimal subthreshold characteristics, dual doped poly-Si gates (N^+ poly for NMOS and P^+ poly for PMOS) are typically used. For example, in the 0.25-μm fully depleted SOI CMOS process developed at Lincoln Laboratory, degenerately doped ($>10^{20}$ cm^{-3} As for NMOS and B for PMOS) poly-Si gates with an average channel doping of 3×10^{17} cm^{-3} (B for NMOS and P for PMOS) were implemented to achieve the designed thresholds of +0.4 and –0.4 V for NMOS and PMOS, respectively.

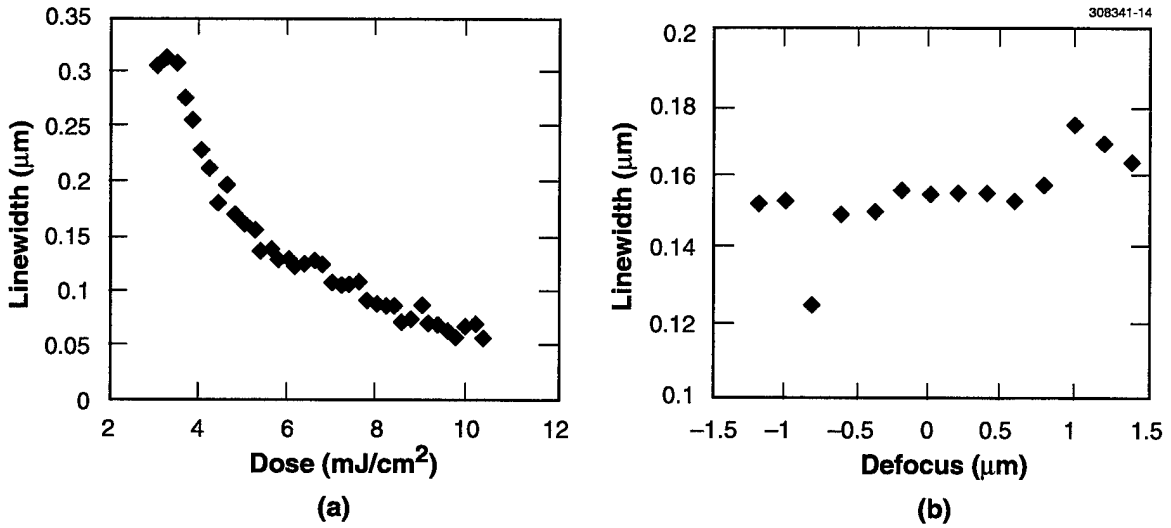

Figure 7-5. Width of an etched line vs (a) dose and (b) defocus. The line patterned in 200-nm-thick polysilicon is defined by phase shift lithography with 248-nm wavelength using 320-nm-thick UV-5 photoresist.

However, as one continues to scale down the channel length and the overall device dimensions in the SOI CMOS technology, it is also necessary to reduce the SOI and the buried oxide thickness to minimize the short-channel effect, i.e., the two-dimensional field coupling between the drain and the channel of a transistor. Consequently, it becomes increasingly difficult to control the threshold voltage with channel doping. By simple consideration of the one-dimensional Poisson's equation for a fully depleted SOI layer, one finds that the contribution of the SOI depletion charge to the threshold is $qN_At_{SOI}/2C_{ox}$, where N_A is the average doping concentration in the SOI layer, t_{SOI} is the SOI thickness, and C_{ox} is the front gate oxide capacitance. For a fully depleted 25-nm gate length SOI CMOS transistor to be functional, ultrathin gate oxide and SOI layer are required (<3 nm for gate oxide and <5 nm for SOI). With such thickness, even a 10^{18} cm^{-3} doping only contributes less than 0.03 V to the threshold. Therefore, choosing a proper gate workfunction for controlling the flatband voltage is more effective in setting the overall threshold voltage. For symmetrical CMOS, midgap gate material provides the optimum workfunction (4.61 eV). With the one-dimensional analytical model developed by Lim and Fossum [3], one can estimate the threshold voltage for a fully depleted SOI CMOS device, as illustrated in Figure 7-6. As expected, with a midgap gate, the thresholds are symmetrical for NMOS and PMOS. Moreover, they become less dependent on the channel doping as the SOI thickness is reduced.

Titanium nitride is a promising material for achieving the desired workfunction. Several workers had successfully implemented this material as gate electrode in their larger gate length (>0.5 μm) CMOS process [4],[5]. TiN gate offers several key advantages compared to the conventional poly-Si gate. Besides having the right workfunction for symmetrical CMOS characteristics, TiN has relatively low resistivity

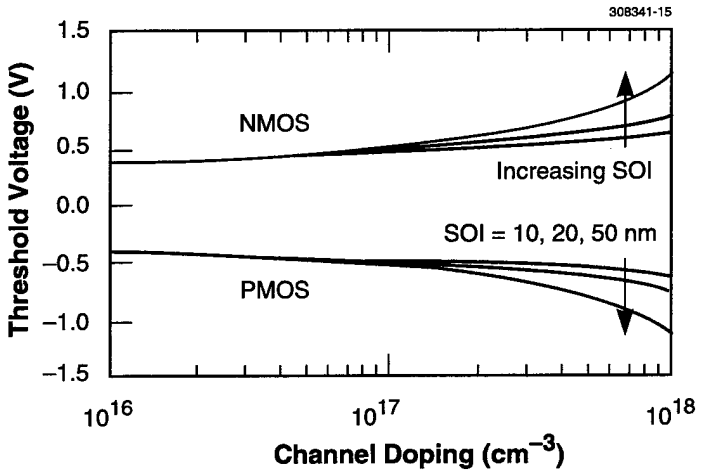

Figure 7-6. Fully depleted SOI CMOS threshold voltage for midgap gate. The threshold voltages were calculated as a function of the channel doping for midgap gate material with a workfunction of 4.61 eV using the one-dimensional Lim-Fossum analytical model [3]. There are three sets of curves for NMOS and PMOS, each representing a different SOI thickness (10, 20, and 50 nm). The interface fixed charge was assumed to be 5×10^{10} cm^{-2}.

(~60 to 80 $\mu\Omega$ cm) and is a good diffusion barrier. The low resistivity is especially important for fully depleted SOI CMOS technology, because it allows one to optimize the thin source/drain silicide for low contact resistance without sacrificing the gate sheet resistance.

To verify the midgap characteristics of TiN, we have fabricated simple MOS capacitors with reactively sputtered TiN deposited by the Electrotech Sigma system at Lincoln Laboratory. Both the gate oxide breakdown and the capacitance-voltage (C-V) characteristics were measured for these MOS capacitors. The results for a typical 100-nm-thick TiN on 8-nm-thick gate oxide system are shown in Figure 7-7. For comparison, we also included the results from conventional poly-Si gates. The breakdown measurements indicate that TiN does not degrade the gate oxide breakdown field, still in excess of 10 MV/cm for 8-nm gate oxide. Moreover, the C-V characteristics for *n*- and *p*-type substrates are symmetrical about 0 V, which suggests that the workfunction of TiN is indeed close to midgap.

As a part of the process integration for fabricating the SOI CMOS, it is also necessary to study the thermal stability of the TiN gate. In a self-aligned source/drain fabrication process, the TiN gate needs to be subjected to a high-temperature (>850°C) rapid thermal anneal (RTA) for activating the dopants in the source/drain regions. To investigate this problem, we have subjected the TiN MOS capacitors to RTA in N_2 ambient with temperatures ranging from 475 to 950°C. The results are shown in Figure 7-8. The TiN film clearly exhibits significant changes both in sheet resistivity and the flatband voltage of MOS capacitors when the RTA temperature exceeds 700°C.

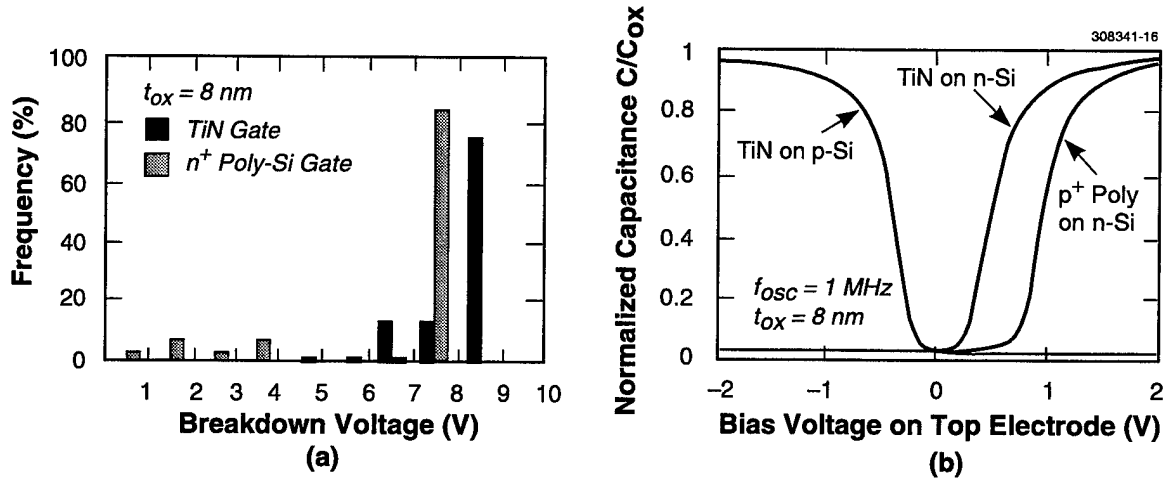

Figure 7-7. (a) Gate oxide breakdown and (b) high-frequency capacitance-voltage (C-V) characteristics of TiN MOS capacitors. The gate oxide breakdown voltages were measured by the critical voltage required to trigger a 1-μA current flow. The flatband voltages extracted from the C-V curves are –0.22 and 0.35 V for the p-type (doping 7×10^{14} cm^{-3}) and the n-type (doping 1.8×10^{15} cm^{-3}) substrate, respectively. The extracted fixed charge density Q_{ss} for the TiN gate is -1.5×10^{11} cm^{-2}, assuming 4.61-eV midgap workfunction for the TiN. All capacitors have an area of 3×10^{-3} cm^2. The 100-nm-thick TiN was deposited at a substrate temperature of 400°C.

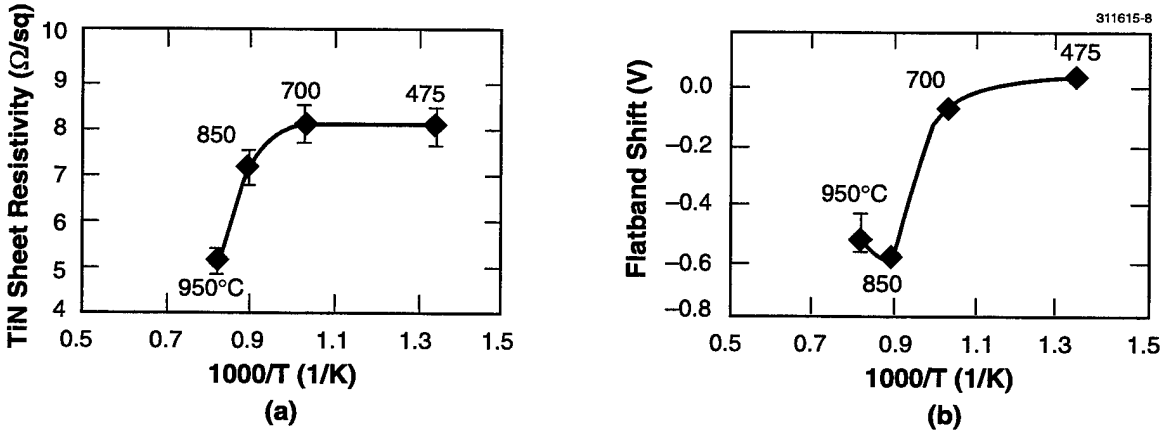

Figure 7-8. Rapid thermal anneal (RTA) induced changes in TiN MOS capacitors. The (a) TiN (100 nm thick) sheet resistivity and (b) MOS capacitors' flatband voltage shifts relative to the unannealed sample are plotted as functions of the RTA temperature. The RTA was performed in N_2 ambient at a given temperature for 30 s using an AG Heatpulse 4100 system. The TiN sheet resistivity was measured by a Prometrix 4-point probe system.

The sheet resistivity change is favorable for the final device performance. For a 100-nm-thick film, it decreases from 8 to 5 Ω/sq after a 950°C, 30-s anneal in 100% N_2 ambient. It is important that this annealing be done in a nonoxidizing ambient, because TiN can be oxidized easily and the oxide is highly resistive. The drop in sheet resistivity with annealing is most likely the result of TiN grain growth.

A more troubling change with the RTA processing is the flatband voltage of the TiN MOS capacitors. Although there is no significant change in the gate oxide breakdown characteristics and the effective oxide thickness, the flatband voltage shifts in the negative direction by as much as 0.6 V after annealing at a temperature greater than 850°C (see Figure 7-8). This large shift occurs in both *p*- and *n*-type substrates. Moreover, it is independent of the TiN film thickness (50–100 nm) and the TiN deposition substrate temperature (150–550°C). Putting a 100-nm-thick plasma-enhanced chemical vapor deposition (PECVD) TEOS capping layer on top of the TiN also did not prevent the flatband shift.

A possible cause for the flatband voltage shift with high-temperature annealing is the change of workfunction near the TiN/gate oxide interface. Workfunction studies of Ti interacting with oxygen in ultrahigh vacuum using the Kelvin vibrating capacitor method indicate that the Ti workfunction can decrease as much as 0.8 eV in various oxidized states [6]. This workfunction decrease is consistent with the magnitude and the sign of flatband voltage shift observed in the high-temperature annealed samples. We have also performed Auger analysis on the TiN MOS system. Preliminary results suggest that there is interaction between the TiN and the gate oxide after the high-temperature RTA (850°C, 30 s). More study is needed to resolve this issue. One cannot rule out the possibility of fixed charge creation during the RTA processing, although the fixed charge magnitude required to explain the flatband shift is on the order of 2×10^{12} cm^{-2}. It has been shown that rapid thermal nitridation in NH_3 can cause positive fixed charge as high as 8×10^{11} cm^{-2} [7]. Therefore, it is also important to examine possible contamination during the RTA processing. Currently, we are investigating various approaches to overcome the C-V shift problem. These include replacing the SiO_2 gate dielectric with Si_3N_4, depositing a thin (<10 nm) amorphous Si layer underneath the TiN to form Ti silicide, and capping the TiN with poly-Si [5].

Another major task in developing the midgap gate for the scaled SOI CMOS technology is the gate patterning process. As a part of this effort, we have developed a damascene technique that can be incorporated easily into the SLOTFET CMOS process. As discussed above, the basic concept of the SLOTFET is to construct the Si channel and the gate in a slot etched into a sacrificial layer on top of the SOI. This process allows one to independently optimize the SOI channel thickness for suppressing short-channel effect and the source/drain Si thickness for low contact-resistance silicide formation. The key steps involved in the gate formation are illustrated in Figure 7-9.

To validate this gate fabrication approach, we have implemented the key steps of this damascene process on bare silicon test wafers. After the slot definition and etch in the nitride/oxide sacrificial stack and the SOI channel thinning, LPCVD nitride was used to form sidewall spacers to obtain the desired gate dimensions and to protect the oxide from subsequent cleaning and gate oxidation. With the channel defined and the gate oxide grown, the slot was then filled with TiN by collimated reactive sputtering. The unwanted gate material in the field regions was then removed by chemical mechanical polishing (CMP). Finally, the

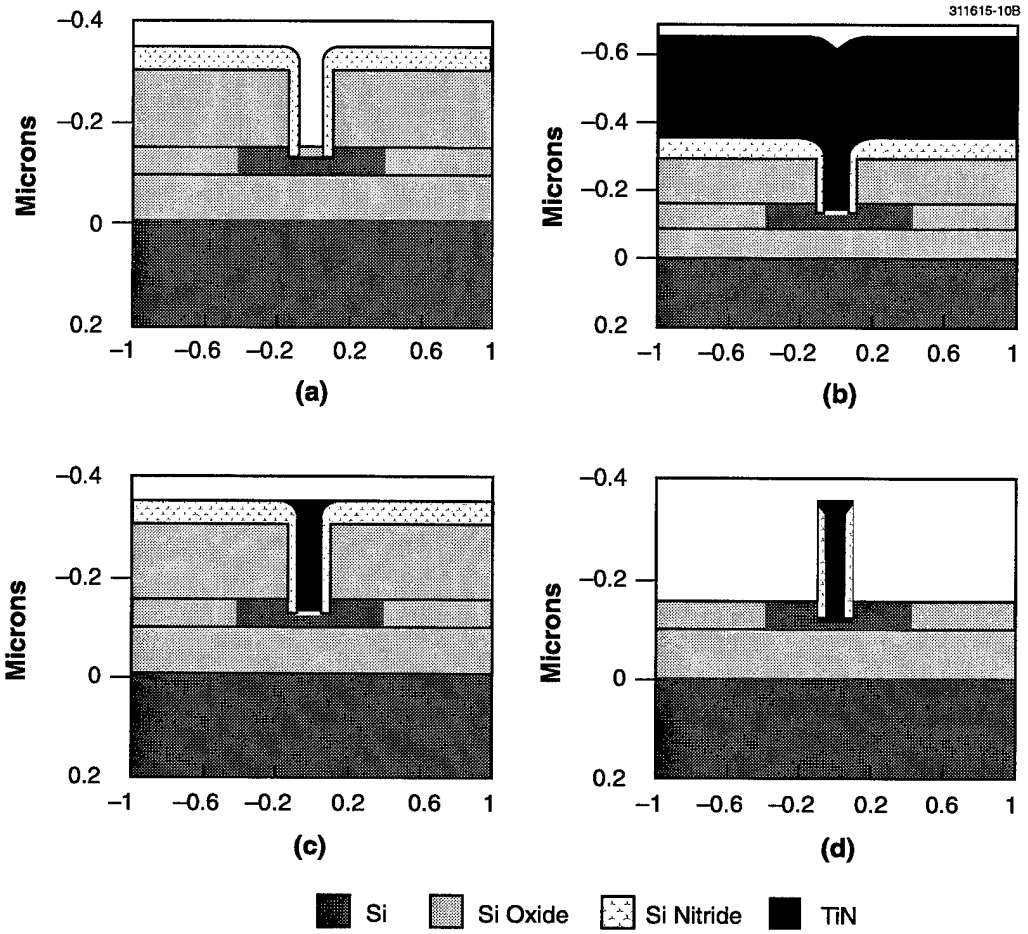

Figure 7-9. Key steps in midgap gate formation process: (a) gate oxidation, (b) TiN deposition, (c) TiN chemical mechanical polishing (CMP), and (d) etchback. These gate formation steps are parts of the overall SLOTFET SOI CMOS process. The device structures were constructed by SILVACO's Athena process simulator.

gate material itself was used as a self-aligned mask for etching away the sacrificial molding material. TiN is a very effective etch stop for oxide, nitride, and Si in any fluorine- and chlorine-based RIE chemistry. After the etchback process, the midgap gate is defined, and the source/drain regions can be accessed for subsequent doping, silicidation, and metallization. The key advantage of this damascene technique is that it allows one to pattern fine TiN gate without direct etching, which was found to be difficult in previous studies [4],[5].

We have applied this technique with high-resolution 193-nm optical lithography to define sub-50-nm TiN "gates." In this experiment, a conventional Cr mask was used to define a 0.2-μm slot in a single-layer

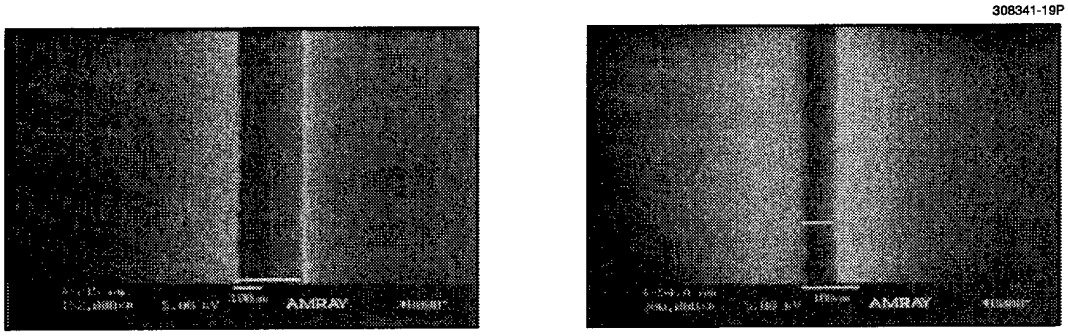

Figure 7-10. Slot formation by high-resolution optical lithography and spacer narrowing. The scanning electron micrographs (SEMs) show (a) the starting slot patterned by the 193-nm lithography system (SVG Micrascan) and then etched down to the underlying sacrificial oxide layer at Lincoln Laboratory, and (b) further narrowing by a 100-nm nitride spacer formation process. The slot etch was done in a LAM Rainbow reactive ion etching system with CF_4/Ar chemistry.

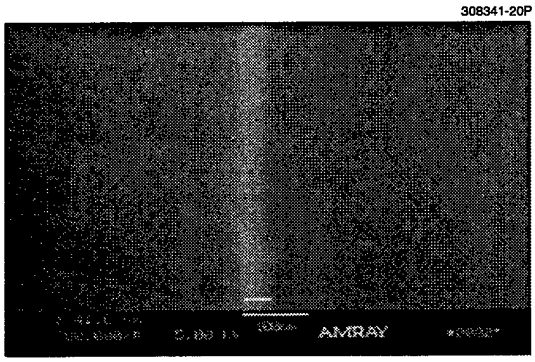

Figure 7-11. 40-nm TiN gate formed by damascene. This SEM shows the final standing 40-nm TiN gate after CMP and subsequent self-aligned etchback of the sacrificial stack.

IBM v. 2.1 193-nm resist (thickness 316 nm). As illustrated in Figure 7-10, this pattern was then transferred into a 150-nm low-pressure chemical vapor deposition (LPCVD) oxide layer with CF_4/Ar reactive ion etching (RIE). The slot was then narrowed by a 100-nm LPCVD nitride spacer, which reduced the width to near 50 nm. Finally, after the collimated TiN deposition and the subsequent CMP process, the sacrificial nitride/oxide stack was etched away with the same RIE chemistry that formed the slot. The final standing TiN strip, shown in Figure 7-11, has a width of 40 nm, which is already close to the 25-nm goal that we are trying to achieve ultimately. Currently, we are working to integrate this gate formation technique into a complete SLOTFET SOI CMOS process.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 November 1997	Quarterly Technical Report, 1 August–31 October 1997

4. TITLE AND SUBTITLE

Solid State Research

5. FUNDING NUMBERS

C — F19628-95-C-0002
PE — 63250F
PR — 221

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Lincoln Laboratory, MIT
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Lexington, MA 02173-9108

8. PERFORMING ORGANIZATION REPORT NUMBER

1997:4

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

HQ Air Force Materiel Command
AFMC/STSC
Wright-Patterson AFB, OH 45433-5001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

ESC-TR-97-097

11. SUPPLEMENTARY NOTES

None

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 August–31 October 1997. The topics covered are Electrooptical Devices, Quantum Electronics, Materials Research, Submicrometer Technology, High Speed Electronics, Microelectronics, and Analog Device Technology. Funding is provided primarily by the Air Force, with additional support provided by the Army, DARPA, Navy, BMDO, NASA, and NIST.

14. SUBJECT TERMS

quantum electronics	high-speed electronics	epitaxial growth	charge-coupled devices
electro-optical devices	microelectronics	lasers	resistor fabrication
materials research	analog device technology	optical lithography	field-effect transistors
submicrometer technology	advanced silicon technology		

15. NUMBER OF PAGES 78

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Same as Report	Same as Report	Same as Report